reviewer4@nptel.iitm.ac.in ▼ Courses » Computer Organization and Architecture A Pedagogical Aspect Announcements Course Ask a Question **Progress** FAQ Unit 6 - Week 5: **Addressing Modes, Instruction Set and Instruction Execution Flow** Register for **Assignment for Week 5 Certification exam** The due date for submitting this assignment has passed. Course As per our records you have not submitted this Due on 2019-03-06, 23:59 IST. outline assignment. 1) JU 3F3F: This instruction causes the program to jump to location 3F3F unconditionally. JU 1 point How to access the portal Week 1: Data transfer instruction **Fundamentals of** Control instruction **Digital Computer** Arithmetic and Logical instruction Week 2: Hybrid Instruction Fundamental of Digital Computer No, the answer is incorrect. Week 3: Addressing **Accepted Answers:** Modes. Control instruction Instruction Set and Instruction 2) JUZ 3F3F: This instruction causes the program to jump to location 3F3F if Zero flag is set. 1 point **Execution Flow** JUZ is a Week 4: Data transfer instruction Addressing Modes, Un-conditional Control instruction **Instruction Set** Conditional Control instruction and Instruction **Execution Flow** None of the above Week 5: No, the answer is incorrect. Addressing Score: 0 Modes, **Accepted Answers:** Instruction Set Conditional Control instruction and Instruction **Execution Flow** 3) Assume that we have a 4 bit ALU. Consider the operation 5 + 2 given below, assuming 1 point Lecture 1: signed arithmetic © 2014 NPTEL - Privacy & Terms - Honor Code - FAQs -In association with A project of

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Quiz :	5+2: Assumed signed arithmetic
Assignment for Week 5	5 is represented as 0101 in 2's complement format 1 is represented as 0010 in 2's complement format
Week 6:	Now, 0101
Organization	+ 0010
and Optimization	0111
of Micro-	
programmed	
Controlled	After the operation, which of the following options denote the values of the flags: Zero, Negative, Carr
Control Unit	Even Parity?
Week 7:	7 Januari Manathina 1 Communi and Fivon Positive 1
Organization	Zero=1, Negative=1, Carry=1, and Even Parity =1
and Optimization	Zero=0, Negative=1, Carry=0, and Even Parity =0
of Micro-	Zero=0, Negative=0, Carry=0, and Even Parity =0
programmed	Zero-o, Negative-o, Carry-o, and Everi Parity -o
Controlled Control Unit	Zero=1, Negative=0, Carry=0, and Even Parity =1
	No, the answer is incorrect.
Week 8:	Score: 0
Organization and Optimization	Accepted Answers:
of Micro-	Zero=0, Negative=0, Carry=0, and Even Parity =0
programmed	
Controlled	4) What will be the value in R0 after executing the following sub-program? 1 poin
Control Unit	MOV// PO 00
	MOVI R0, 00
Week 9: Memory	While:
Sub-system Organization	ADDI R0, 10 // R0 = R0 + 10
Organization	CMPI R0, 50 // Compare value in R0 with 50 (immediate value)
Week 10:	JNE While // Jump to While if the value in R0 is not equal to 50.
Memory	0 10
Sub-system	10
Organization	20
	© 50
Week 11:	
Memory Sub-evetem	None of the above
Sub-system Organization	No, the answer is incorrect.
	Score: 0
Week 12:	
Input/output	Accepted Answers:
Subsystem	50
TEXT TRANSCRIPTS	5) In nested procedure CALL/RETURN, prior to the starting of a subroutine, which of the following is performed?
	PC (Program Counter), PSW (Program Status Word) register variables etc. are retrieved
	from the queue
	PC (Program Counter), PSW (Program Status Word) register variables etc. are retrieved
	from the stack
	PC (Program Counter), PSW (Program Status Word) register variables etc. are saved in a
	queue
	PC (Program Counter), PSW (Program Status Word) register variables etc. are saved in a
	stack
	No, the answer is incorrect.
	Score: 0
	Accepted Answers:
	PC (Program Counter), PSW (Program Status Word) register variables etc. are saved in a stack
	6) The following is the micro-operation sequence needed for the instruction PUSH: 1 poin

PUSH Ri				
a.	MAR ← SP			
b. c.	Write			
d.	SP=SP-1 // Decrement the stack pointer value			
Which of the following describes most appropriately, the second step?				
	PC ← PC+1 (PC gets incremented by instruction length)	R		
	MAR ← address of operand in IR			
	PC ← Pop the return address from the stack	C///		
	■ MBR ← Ri			
	lo, the answer is incorrect. Score: 0	<u>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</u>		
Δ	Accepted Answers:			
٨	MBR ← Ri			
7) The following is the micro-operation sequence needed for the instruction 'POP': 1 point POP Ri				
a:	SP <- SP +1			
b:				
c: d:	Read Ri <- MBR // pop the top element of stack and store in register Ri			
<u>.</u>	u. The MBK // popule top element of stack and store in register hi			
Which of the following describes most appropriately, the second step (i.e., is (b)) marked above with				
	PC<-PC+1 (PC gets incremented by instruction length)			
MAR <- address of operand in IR PC <-Pop the return address from the stack				
MAR <-SP (Memory address register is assigned the value of Stack Pointer)				
No, the answer is incorrect. Score: 0				
Accepted Answers:				
٨	MAR <-SP (Memory address register is assigned the value of Stack Pointer)			
8)	The overflow bit is SET if	. point		
	If the sum of 2 positive numbers yields a positive number			
	If the addition of 2 numbers result in carry out of the most significant number			
	If the sum of 2 positive numbers yields a negative number			
	None of the above			
	lo, the answer is incorrect. Score: 0			
	Accepted Answers: f the sum of 2 positive numbers yields a negative number			
9)	A stack pointer gives	l point		
	The address of the memory of the stack where the details of the main program is stored	d.		
The address of the PSW and PC of the currently executing subroutine.				
	The address of the last filled memory of the stack after each subroutine call.			
	None of the above			

