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Courses » Computer Organization and Architecture A Pedagogical Aspect

Announcements **Course** Ask a Question Progress FAQ

Unit 5 - Week 4: Addressing Modes, Instruction Set and Instruction Execution Flow

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Course outline

Assignment for Week 4

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-02-27, 23:59 IST.

1) An instruction SUB 3030 ***1 point***

- Subtracts 3030 to the value in Accumulator and stores the result in the memory location 3030
- Subtracts the value in memory location 3030 to the value in Accumulator and stores the result in Accumulator
- Subtracts 3030 to the value in Accumulator and stores the result in Accumulator
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Subtracts the value in memory location 3030 to the value in Accumulator and stores the result in Accumulator

2) The instruction ADD 3030 is of ***1 point***

- A 3-address instruction format
- A 2-address instruction format
- A 1-address instruction format
- A 0-address instruction format

No, the answer is incorrect.
Score: 0

Accepted Answers:
A 1-address instruction format

3) STORE R1, 3030 is ***1 point***

Score: 0

Accepted Answers:

Data transfer instruction

4) Which of the following options represents the correct matching? ***1 point***

Addressing Mode	Description
1. Immediate	A. the address field refers to the address of a word in the memory, which in-turn contains the address of the operand
2. Direct	B. the address field contains the address (in main memory) where the operand is stored
3. Indirect	C. operand value is present in the instruction itself (address field)
4. Register Direct	D. the address field of the operand is a register

- 1->A; 2->D; 3->C; 4->B;
- 1->C; 2->B; 3->D; 4->A;
- 1->C; 2->B; 3->A; 4->D;
- 1->A; 2->D; 3->B; 4->C;

No, the answer is incorrect.

Score: 0

Accepted Answers:

1->C; 2->B; 3->A; 4->D;

5) Consider an example of memory organization as shown in the figure below. Which value will be loaded into the accumulator when the instruction “LOAD DIRECT 3” is executed? ***1 point***

Memory Location address	0	1	2	3	4	5	6	7
Content	10	23	25	20	12	3	1	2

- 3
- 25
- 12
- 20

No, the answer is incorrect.

Score: 0

Accepted Answers:

20

6) As per the example shown in the previous question (question 5), what will be the content of the accumulator when the instruction “LOAD INDIRECT 7” is executed? ***1 point***

- 2
- 25
- 7
- 20

No, the answer is incorrect.

Score: 0

Accepted Answers:

25

7) For a 0-address instruction format, what would be the top element of the stack following sequences of instructions? ***1 point***

PUSH 20; PUSH 5; PUSH 5; ADD; SUB; PUSH 20; MULT.

- 100
- 200
- 10
- 5

No, the answer is incorrect.
Score: 0

Accepted Answers:
200

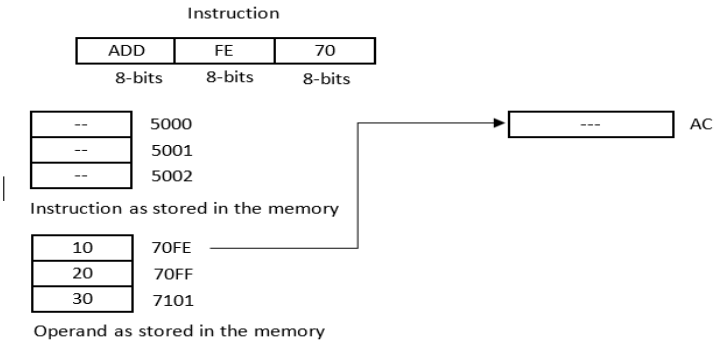
8) How many bits of opcode is required to implement a CPU with 10 arithmetic and logical instructions, 2 control instructions, and 5 data transfer instructions? ***1 point***

- 2
- 3
- 4
- 5

No, the answer is incorrect.
Score: 0

Accepted Answers:
5

9) Consider a CPU with 8-bit data bus and 16-bit address bus. The memory is byte organized. Consider the instruction format with one operand. Length of the instruction is three bytes and the first byte indicates the op-code. Second byte indicates the lower eight bits address and third byte indicates the higher eight bits address. Consider the instruction “ADD FE 70”. This instruction adds the content of memory location to accumulator. The instruction is stored in consecutive memory location starting from memory location 5000H. We assume that Accumulator initially has the value of 20. In the figure given below, what are the values in Memory Locations 5000, 5001, 5002 and Accumulator after the instruction ADD FE 70 is executed. ***1 point***

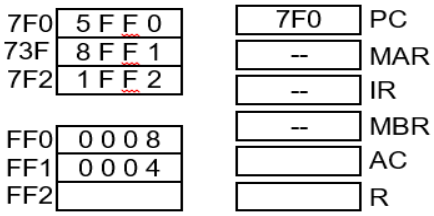


- 5000=ADD, 5001=FE, 5002=70, and Accumulator=30
- 5000=ADD, 5001=70, 5002=FE, and Accumulator=30
- 5000=ADD, 5001=70, 5002=FE, and Accumulator=40
- 5000=ADD, 5001=FE, 5002=70, and Accumulator=40

No, the answer is incorrect.
Score: 0

Accepted Answers:
5000=ADD, 5001=FE, 5002=70, and Accumulator=30

10) The instruction LDA FF0 (machine code of LDA is 5) is stored in location 7F0. The contents in memory location FF0 are loaded into accumulator. After its execution, accumulator stores value 8. The figure below shows a snapshot of the registers and their contents. ***1 point***



Immediately after the fetch cycle of the 1st instruction (LDA FF0), the values in MAR, IR and MBR are:

- MAR=FF0, IR=5FF0, MBR=5FF0
- MAR=7F0, IR=5FF0, MBR=0008
- MAR=7F0, IR=5FF0, MBR=5FF0
- MAR=FF1, IR=5FF0, MBR=7F0

No, the answer is incorrect.
Score: 0

Accepted Answers:
MAR=7F0, IR=5FF0, MBR=5FF0

Previous Page End