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Courses » Computer Organization and Architecture A Pedagogical Aspect

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Unit 4 - Week 3: Addressing Modes, Instruction Set and Instruction Execution Flow

Register for Certification exam

Course outline

Assignment for Week 3

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-02-20, 23:59 IST.

1) Component of CPU which is responsible for comparing contents of two pieces of data is *1 point*

- ALU
- CU
- Memory
- Register

No, the answer is incorrect.
Score: 0

Accepted Answers:
ALU

2) A CPU has 16 bit program counter. This means that the CPU can address *1 point*

- 16K memory locations
- 32K memory locations
- 64K memory locations
- 256K memory locations

No, the answer is incorrect.
Score: 0

Accepted Answers:
64K memory locations

3) CPU gets the address of next instruction to be processed from *1 point*

- Instruction register
- Memory address register

Program counter

4) On getting an interrupt, CPU **0 points**

- finishes the current instruction and moves to interrupt service routine
- immediately moves to interrupt service routine without completing current instruction
- releases the control on I/O lines and memory lines
- makes the peripheral device, which requested the interrupt wait for fixed interval of time

No, the answer is incorrect.
Score: 0

Accepted Answers:
immediately moves to interrupt service routine without completing current instruction

5) The module which is not part of CPU: **1 point**

- Arithmetic processing unit
- General purpose registers
- Main memory
- Control unit

No, the answer is incorrect.
Score: 0

Accepted Answers:
Main memory

6) Suppose the size of the Main Memory is 16K * 8 bits. What are the sizes of address bus and data bus? **1 point**

- Address bus = 16 bits, Data bus = 8 bits
- Address bus = 14 bits, Data bus = 3 bits
- Address bus = 16 bits, Data bus = 3 bits
- Address bus = 14 bits, Data bus = 8 bits

No, the answer is incorrect.
Score: 0

Accepted Answers:
Address bus = 14 bits, Data bus = 8 bits

7) How many memory chips of configuration 1K x 8 Bits are required to implement an 8K x 32 Bits memory? **1 point**

- 4
- 8
- 16
- 32

No, the answer is incorrect.
Score: 0

Accepted Answers:
32

8) How many bits are transferred in one memory cycle if the MBR is 64 Bit? **1 point**

- 32
- 64
- 128

256

No, the answer is incorrect.
Score: 0

Accepted Answers:
64

9) The return address from the interrupt-service routine is stored on ***1 point***

- System heap
- Processor register
- Processor stack
- None of the Above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Processor stack

10When a user starts a program, it is: ***1 point***

- loaded into the CPU
- erased from the hard drive.
- loaded into RAM.
- temporarily removed from the registers

No, the answer is incorrect.
Score: 0

Accepted Answers:
loaded into RAM.

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