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Unit 3 - Week 2: Fundamental of Digital Computer

Register for Certification exam

Course outline

How to access the portal

Week 1: Fundamentals of Digital Computer

Week 2: Fundamental of Digital Computer

- Lecture 1: Basic Elements of Processor
- Lecture 2: Storage and I/O Interface
- Lecture 3: Execution of Program and Programming Languages
- Quiz : Assignment for Week 2

Week 3: Addressing Modes, Instruction Set and Instruction Execution Flow

Assignment for Week 2

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment. **Due on 2019-02-13, 23:59 IST.**

1) During a fetch-execute cycle, the memory address of the instruction to be fetched is transmitted from the program counter to the RAM through _____. ***1 point***

- Data bus
- Address bus
- Control bus
- Either (a) or (b)

No, the answer is incorrect.
Score: 0

Accepted Answers:
Address bus

2) Choose the sequence appropriately to fill the blank space. _____ holds the memory address of the data needing to be accessed by the CPU. _____ holds the data being transferred to or from the memory location by the CPU. _____ holds the memory address of the next instruction to be executed. _____ holds the result of a calculation performed by the arithmetic/logic unit. ***1 point***

- PC, MAR, MDR, ACC
- MAR , PC, MDR, ACC
- PC, ACC, MDR, MAR
- MAR, MDR, PC, ACC

No, the answer is incorrect.
Score: 0

Accepted Answers:
MAR, MDR, PC, ACC

- 28

No, the answer is incorrect.
Score: 0

Accepted Answers:
31

4) A processor can support a maximum memory of 4 GB, where the memory is word addressable (a word consists of 1 byte). The size of the address bus of the processor is at least _____ bits. ***1 point***

- 32
- 31
- 30
- 29

No, the answer is incorrect.
Score: 0

Accepted Answers:
32

5) A processor has 24-bit data bus and 32-bit address bus. Calculate the amount of memory that can address by this computer. ***1 point***

- 32GB
- 16GB
- 12GB
- 10GB

No, the answer is incorrect.
Score: 0

Accepted Answers:
12GB

6) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. How many bits are there in the operation code, the register code part, and the address part respectively? ***1 point***

- 8, 8, 17
- 9, 8, 18
- 7, 6, 18
- 7, 7, 17

No, the answer is incorrect.
Score: 0

Accepted Answers:
7, 6, 18

7) If the last operation performed on a computer with an 8-bit word was a subtraction (A-B) in which the two operands were A=11110000 and B=0010100, what would be the value of Carry, Zero, Overflow, Sign, Even Parity, and Half Carry flags? Assume that, the operands are stored in sign magnitude form. [Hints: Use 2's complement subtraction method]. ***1 point***

- 0, 0, 1, 0, 1, 0
- 0, 1, 0, 0, 1, 0
- 0, 0, 0, 0, 1, 0

- 1, 0, 0, 1, 0, 0

No, the answer is incorrect.
Score: 0

Accepted Answers:
1, 0, 0, 1, 0, 0

8) Assume that we have a 4-bit ALU. For the operation 5+ (-5) (assumed signed arithmetic), what are the value of Zero, Negative, Carry, Overflow, and Even Parity flags. [Hints: Use 2's complement arithmetic] ***1 point***

- 0, 1, 1, 1, 0
- 1, 0, 1, 0, 1
- 1, 0, 1, 1, 1
- 1, 1, 1, 0, 1

No, the answer is incorrect.
Score: 0

Accepted Answers:
1, 0, 1, 0, 1

9) A processor has 40 distinct instructions and 24 general purpose register. A 32-bit instruction word has an opcode, two registers operand, and an immediate operand. The number of bits available for the immediate operand field is _____. ***1 point***

- 16
- 12
- 8
- 10

No, the answer is incorrect.
Score: 0

Accepted Answers:
16

10) An instruction ADD R1, A is stored at memory location 4004H. R1 is a processor register and A is a memory location with address 400CH. Each instruction is 32-bit long. What will be the values of PC, IR and MAR during execution of the instruction? ***1 point***

- 4004H; ADD R1, A; 400CH
- 4008H; ADD R1, A; 400CH
- 4008H; ADD; 400CH
- 4008H; ADD R1, A; 432CH

No, the answer is incorrect.
Score: 0

Accepted Answers:
4008H; ADD R1, A; 400CH

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