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Courses » Computer Organization and Architecture A Pedagogical Aspect

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Unit 13 - Week 12: Input/output Subsystem

Register for Certification exam

Course outline

How to access the portal

Week 1: Fundamentals of Digital Computer

Week 2: Fundamental of Digital Computer

Week 3: Addressing Modes, Instruction Set and Instruction Execution Flow

Week 4: Addressing Modes, Instruction Set and Instruction Execution Flow

Week 5: Addressing Modes, Instruction Set and Instruction Execution Flow

Week 6: Organization and Optimization

Assignment for Week 12

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment. **Due on 2019-04-24, 23:59 IST.**

Assignment for Week 12

1) Mark whichever is correct for Memory mapped I/O scheme. ***1 point***

- [ ] The I/O device and the memory have separate address space.
- [ ] The I/O device and the memory shares same address space.
- [ ] No special command for I/O is needed
- [ ] Needs I/O or memory select line

No, the answer is incorrect.
Score: 0

Accepted Answers:
The I/O device and the memory shares same address space.
No special command for I/O is needed

2) In _____ mode, the I/O module and main memory exchange data directly, without processor involvement. ***1 point***

- ( ) Programmed I/O
- ( ) DMA
- ( ) Interrupt-driven I/O
- ( ) All the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
DMA

3) Which method among these uses interrupt to transfer data from I/O to memory. ***1 point***

Score: 0

Accepted Answers:
Interrupt-driven I/O
DMA

4) A CPU generally handles an interrupt by executing an interrupt service routine ***1 point***

- As soon as an interrupt is raised
- By checking the interrupt register at the end of fetch cycle
- By checking the interrupt register after finishing the execution of the current instruction
- By checking the interrupt register at fixed intervals.

No, the answer is incorrect.
Score: 0

Accepted Answers:
By checking the interrupt register after finishing the execution of the current instruction

5) A DMA module is transferring characters (8-bit) to memory using cycle stealing from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity? ***1 point***

- 0.10%
- 0.12%
- 0.24%
- 0.5%

No, the answer is incorrect.
Score: 0

Accepted Answers:
0.12%

6) The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____. ***1 point***

- 675
- 456
- 3246
- 2915

No, the answer is incorrect.
Score: 0

Accepted Answers:
456

7) Suppose a given bus protocol requires 10ns for devices to make requests, 15ns for arbitration, and 25ns to complete each operation. How many operations can be completed per second? ***1 point***

- 15 million/sec
- 10 million/sec
- 20 million/sec
- 18 million/sec

No, the answer is incorrect.
Score: 0

Accepted Answers:
20 million/sec

8) A hard disk with 5 platters has 2048 tracks/platter, 1024 sectors/track (fixed number of sectors per track), and 512 byte sectors. What is its total capacity? ***1 point***

- 7GB
- 5GB
- 4GB
- 8GB

No, the answer is incorrect.
Score: 0

Accepted Answers:
5GB

9) A manufacturer wishes to design a hard disk with a capacity of 30 GB or more (using the standard definition of 1GB = 2^30 bytes). If the technology used to manufacture the disks allows 1024-byte sectors, 2048 sectors/track, and 4096 tracks/platter, how many platters are required? (Assume a fixed number of sectors per track.) ***1 point***

- 3
- 5
- 4
- 2

No, the answer is incorrect.
Score: 0

Accepted Answers:
4

10) A hard disk with one platter rotates at 15,000 r/min and has 1024 tracks, each with 2048 sectors. The disk head starts at track 0 (tracks are numbered from 0 to 1023). The disk then receives a request to access a random sector on a random track. If the seek time of the disk head is 1 ms for every tracks it must cross. What is the transfer time for a sector? ***1 point***

- 1.95 microseconds
- 2.5 microseconds
- 2 microseconds
- 3 microseconds

No, the answer is incorrect.
Score: 0

Accepted Answers:
1.95 microseconds

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