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Unit 10 - Week 9: Memory Sub-system Organization

Register for Certification exam

Course outline

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Assignment for Week 9

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-04-03, 23:59 IST.

1) In a two-level cache system, the access times of L1 and L2 are 1 and 8 clock cycles, respectively. The miss penalty of L2 cache is18 clock cycles. The miss rate of L1 cache is twice as that of L2. The average memory access time (AMAT) of this cache system is 2 cycles. What are the miss rates of L1 and L2? ***1 point***

- 0.111 and 0.056
- 0.056 and 0.111
- 0.0892 and 0.1784
- 0.1784 and 0.0892

No, the answer is incorrect.
Score: 0

Accepted Answers:
0.111 and 0.056

2) Consider a 2 level cache system. Access times of L1 cache, L2 cache and main memory are 1 ns, 10ns, and 500 ns, respectively. The hit rates of L1 and L2 caches are 0.8 and 0.9, respectively. If the search time within the cache is not considered, what would be the average access time of the system? ***1 point***

- 13.0 ns
- 12.8 ns
- 12.6 ns
- 12.4 ns

No, the answer is incorrect.
Score: 0

Accepted Answers:
12.6 ns

- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Direct mapping

4) A block-set associative cache memory with 128 blocks are divided into four block sets. The main memory consists of 16,384 blocks where each block contains 256 eight bit words. How many bits are required for addressing the main memory? ***1 point***

- 23
- 22
- 24
- 21

No, the answer is incorrect.
Score: 0

Accepted Answers:
22

5) How many bits are needed to represent the TAG, SET and WORD fields for the same cache organisation mentioned in question 4? ***0 points***

- Word : 8, Set: 6, Tag: 14
- Word : 13, Set: 5, Tag: 8
- Word : 8, Set: 5, Tag: 14
- Word : 8, Set: 5, Tag: 13

No, the answer is incorrect.
Score: 0

Accepted Answers:
Word : 8, Set: 5, Tag: 13

6) In which mapping, the data can be mapped anywhere in the cache memory? ***1 point***

- Associative
- Direct
- Set Associative
- Indirect

No, the answer is incorrect.
Score: 0

Accepted Answers:
Associative

7) The main memory access on a cache "miss" takes 30 ns and a cache access on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time? ***1 point***

- 8.4 ns
- 33 ns
- 24.6 ns
- 27.0 ns

No, the answer is incorrect.
Score: 0

Accepted Answers:
8.4 ns

8) Consider a 8-way set associative mapped cache of size 512 KB with block size 1 KB. The tag field contains 7 bits. What will be the size of the main memory? ***1 point***

- 16MB
- 2MB
- 8MB
- 4MB

No, the answer is incorrect.
Score: 0

Accepted Answers:
8MB

9) Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache? ***1 point***

- Write through
- Write back
- Both write through and write back
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Write back

10) Consider an array A[999] with each element occupying 4 words. A 32 word cache is used and divided into 16 word blocks. What is the miss ratio for the following statement? ***1 point***

```
for(i=0; i < 1000; i++)
 A[i] = A[i] + 99;
```

- 0.375
- 0.250
- 0.500
- 0.125

No, the answer is incorrect.
Score: 0

Accepted Answers:
0.125

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