reviewer4@nptel.iitm.ac.in ▼ Courses » Computer Organization and Architecture A Pedagogical Aspect Announcements Course Ask a Question **Progress** FAQ **Unit 10 - Week 9: Memory Sub-system Organization** Register for **Assignment for Week 9 Certification exam** The due date for submitting this assignment has passed. Course As per our records you have not submitted this Due on 2019-04-03, 23:59 IST. outline assignment. How to access 1) In a two-level cache system, the access times of L1 and L2 are 1 and 8 clock cycles, 1 point the portal respectively. The miss penalty of L2 cache is18 clock cycles. The miss rate of L1 cache is twice as that of L2. The average memory access time (AMAT) of this cache system is 2 cycles. What are the miss Week 1: rates of L1 and L2? Fundamentals of **Digital Computer** 0.111 and 0.056 0.056 and 0.111 Week 2: Fundamental of 0.0892 and 0.1784 **Digital Computer** 0.1784 and 0.0892 Week 3: No, the answer is incorrect. Addressing Modes. Score: 0 **Instruction Set Accepted Answers:** and Instruction 0.111 and 0.056 **Execution Flow** 2) Consider a 2 level cache system. Access times of L1 cache, L2 cache and main memory Week 4: are 1 ns, 10ns, and 500 ns, respectively. The hit rates of L1 and L2 caches are 0.8 and 0.9, Addressing respectively. If the search time within the cache is not considered, what would be the average access Modes, time of the system? Instruction Set and Instruction **Execution Flow** 13.0 ns 12.8 ns Week 5: Addressing 12.6 ns Modes, 12.4 ns Instruction Set and Instruction No, the answer is incorrect. **Execution Flow** Score: 0 Week 6: **Accepted Answers:** Organization 12.6 ns

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and Optimization of Micro-	None of the above
programmed	No, the answer is incorrect.
Controlled Control Unit	Score: 0
	Accepted Answers:
Week 8: Organization and Optimization	Direct mapping  4) A block-set associative cache memory with 128 blocks are divided into four block sets. The 1 point
of Micro- programmed	main memory consists of 16,384 blocks where each block contains 256 eight bit words. How many bi
Control Unit	are required for addressing the main memory?
Week 9: Memory	O 22
Sub-system Organization	24
Basics of	<b>□</b> 21
Memory and	No, the answer is incorrect.
Cache (Part-1)	Score: 0
Basics of Memory and	Accepted Answers:
Cache (Part-2)	22
Direct-mapped Caches:	5) How many bits are needed to represent the TAG, SET and WORD fields for the same acache organisation mentioned in question 4?
Misses, Writes and	Word : 8, Set: 6, Tag: 14
Performance	Word: 13, Set: 5, Tag: 8
Associative and	Word: 8, Set: 5, Tag: 14
Multi-level Caches	
	Word : 8, Set: 5, Tag: 13
Summary	No, the answer is incorrect.
<ul><li>Quiz : Assignment for</li></ul>	Score: 0
Week 9	Accepted Answers:  Word: 8, Set: 5, Tag: 13
Week 10: Memory	6) In which mapping, the data can be mapped anywhere in the cache memory? 1 point
Sub-system Organization	Associative
Mark 44	Direct
Week 11: Memory	Set Associative
Sub-system	Indirect
Organization	
Week 12:	No, the answer is incorrect. Score: 0
Input/output	Accepted Answers:
Subsystem	Associative
TEXT TRANSCRIPTS	7) The main memory access on a cache "miss" takes 30 ns and a cache access on a cache <b>1 point</b> "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average
	memory access time?
	8.4 ns
	33 ns
	24.6 ns
	27.0 ns
	No, the answer is incorrect.
	Score: 0

Accepted Answers: 8.4 ns	
8) Consider a 8-way set associative mapped cache of size 512 KB with block size 1 KB. The tag field contains 7 bits. What will be the size of the main memory?	oint
16MB	
2MB 8MB	₩.
O 4MB	æ
No, the answer is incorrect. Score: 0	
Accepted Answers: 8MB	~~
	200
9) Which cache write mechanism allows an updated memory location in the cache to remain 1 $\mu$ out of date in memory until the block containing the updated memory location is replaced in the cache.	ooint che
Write through	
Write back	
Both write through and write back	
None of the above	
No, the answer is incorrect. Score: 0	
Accepted Answers: Write back	
10)Consider an array A[999] with each element occupying 4 words. A 32 word cache is used and divided into 16 word blocks. What is the miss ratio for the following statement? for (i=0; i < 1000; i++) $A[i] = A[i] + 99;$	ooint
0.375	
0.250	
0.500	
0.125	
No, the answer is incorrect. Score: 0	
Accepted Answers: 0.125	
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