Unit 11 - Week 9

Assignment 9

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-10-02, 23:59 IST.

1) If two transitions from states S0 and S1 have a common next state S2 in an FSM, then: *1 point*

- [ ] It is worth assigning close codes to S0 and S2
- [ ] It is worth assigning close codes to S1 and S2
- [ ] It is worth assigning close codes to S0 and S1
- [ ] It is not worth assigning close codes to any pair out of these states

No, the answer is incorrect.
Score: 0

Accepted Answers:
It is worth assigning close codes to S0 and S1

2) If two transitions to states S0 and S1 have a common present state S2 in an FSM, then it is worth assigning close codes to S0 and S1 *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
TRUE

3) If two transitions from states S0 and S1 have a common next state S2 in an FSM, then which of the following is the best encoding? *1 point*

- [ ] S0 (10000), S1 (11001), S2 (00000)
- [ ] S0 (10000), S1 (11001), S2 (11011)
- [ ] S0 (00000), S1 (00001), S2 (11011)
- [ ] S0 (10000), S1 (11111), S2 (00000)

No, the answer is incorrect.
Score: 0

Accepted Answers:
S0 (00000), S1 (00001), S2 (11011)

4) In the heuristic proposed for the Graph Embedding problem, higher priority is given to the encoding of the states with higher number of outgoing transitions *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
FALSE

5) Retiming of an individual gate (node) can result in: *1 point*

- [ ] Increased area
- [ ] Decreased area
- [ ] Increased clock period requirement
- [ ] Decreased clock period requirement

No, the answer is incorrect.
Score: 0

Accepted Answers:
Increased area
Decreased area
Increased clock period requirement
Decreased clock period requirement

6) In the graph representation of a sequential circuit for retiming optimization, which of the following are true? *1 point*

- [ ] The nodes represent the combinational logic gates.
- [ ] The nodes represent the registers.
- [ ] The edge weights represents the total delay of the combinational gates in a path.
- [ ] The edge weights represent the number of register stages in a path.

No, the answer is incorrect.
Score: 0

Accepted Answers:
The nodes represent the combinational logic gates.
The edge weights represent the number of register stages in a path.

7) In the graph representation used in the Retiming problem, edge weights may become negative after the legal retiming of a node/gate. *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
FALSE

8) In the graph representation used in the Retiming problem, some path delays may be affected by the retiming of a node/gate. *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
FALSE

9) In the graph representation used in the Retiming problem, some path weights may be affected by the retiming of a node/gate. *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
TRUE

10) For sequential circuits, what happens during the retiming optimization that reduces the overall execution time? *1 point*

- [ ] Latency (number of cycles) gets reduced
- [ ] Cycle time (required clock period) gets reduced
- [ ] Both latency and cycle time get reduced
- [ ] Neither latency nor the cycle time is reduced

No, the answer is incorrect.
Score: 0

Accepted Answers:
Cycle time (required clock period) gets reduced