Unit 8 - Week 6

Course outline

How to access the portal

Pre-Course

Week 1

Week 2

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Week 6

- Compiler Transformations in High-level Synthesis:
- Hardware Transformations & ASAP/ALAP Scheduling
- Quiz : Assignment 6
- Feedback Form

Week 7

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Lecture Slides

Assignment 6

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-09-11, 23:59 IST.

1) The loop unrolling transformation exposes parallelism in the specification under what conditions? ***1 point***

- [ ] When the number of iterations is small
- [ ] When there are nested loops
- [ ] When there are independent operations across the iterations
- [ ] When there are memory accesses in the loop body

No, the answer is incorrect.
Score: 0

Accepted Answers:
When there are independent operations across the iterations

2) Assume that the body of a loop requires 10 clock cycles when scheduled, and the loop goes through 6 iterations. Which of the following could be the schedule length of the fully unrolled loop? ***1 point***

- [ ] 10
- [ ] 3
- [ ] 20
- [ ] 60

No, the answer is incorrect.
Score: 0

Accepted Answers:
10
20
60

3) The memory access delay increases if we increase the number of read ports of a memory, keeping the capacity the same ***1 point***

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
TRUE

4) The schedule length of a DFG may decrease if we increase the number of read ports of a memory, keeping the capacity the same ***1 point***

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
TRUE

5) Which of the following is NOT TRUE when the function inlining transformation is applied to a specification? Assume that the FSM combinational logic delay is unaffected ***1 point***

- [ ] It may decrease the size of the intermediate representation
- [ ] It may increase the size of the intermediate representation
- [ ] It may lead to shorter schedules
- [ ] It may lead to longer schedules

No, the answer is incorrect.
Score: 0

Accepted Answers:
It may lead to longer schedules

6) Consider two synthesis solutions: (A) All arrays are stored in a single memory module (B) All arrays are stored in different memory modules ***1 point***

- [ ] A leads to smaller area
- [ ] B leads to smaller area
- [ ] A leads to shorter schedule lengths
- [ ] B leads to shorter schedule lengths

No, the answer is incorrect.
Score: 0

Accepted Answers:
A leads to smaller area
B leads to shorter schedule lengths

7) The Tree Height Reduction transformation always leads to improved performance ***1 point***

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
FALSE

8) The Control Flow to Data Flow transformation primarily targets: ***1 point***

- [ ] Arithmetic constructs
- [ ] Conditional constructs
- [ ] Bit-wise operators
- [ ] Function calls

No, the answer is incorrect.
Score: 0

Accepted Answers:
Conditional constructs

9) The scheduling step in High Level Synthesis results in Operations being mapped to specfic clock cycles ***1 point***

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
TRUE

10) In resource-constrained scheduling: ***1 point***

- [ ] A deadline constraint is given, and the scheduler has to minimise resources used
- [ ] Resources are fixed and the scheduler has to minimise the number of clock cycles
- [ ] Resources are assumed to be infinite, and the scheduler minimises the number of clock cycles
- [ ] A deadline constraint is given and the scheduler has to minimise the number of multiplexors in the datapath

No, the answer is incorrect.
Score: 0

Accepted Answers:
Resources are fixed and the scheduler has to minimise the number of clock cycles

11) When assignment to a variable occurs in some but not all branches of a conditional construct, it can result in inference of a: ***1 point***

- [ ] Multiplexer
- [ ] Complex combinational circuit
- [ ] Latch
- [ ] Decoder

No, the answer is incorrect.
Score: 0

Accepted Answers:
Latch

12) Aggressive loop unrolling might blow up the number of states in the control FSM generated during synthesis ***1 point***

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0

Accepted Answers:
TRUE