Unit 6 - Week 4

Assignment 4

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-08-28, 23:59 IST.

1) Which of the following is an OUTPUT of the High-level Synthesis process? *1 point*

- [ ] HDL description
- [ ] Component library
- [ ] Finite State Machine
- [ ] Datapath

No, the answer is incorrect.
Score: 0
Accepted Answers:
Finite State Machine
Datapath

2) Which of the following are true regarding the FSM and Datapath in High-level Synthesis? *1 point*

- [ ] Control signals are sent by the FSM to the Datapath
- [ ] Control signals are sent by the Datapath to the FSM
- [ ] Status signals are sent by the FSM to the Datapath
- [ ] Status signals are sent by the Datapath to the FSM

No, the answer is incorrect.
Score: 0
Accepted Answers:
Control signals are sent by the FSM to the Datapath
Status signals are sent by the Datapath to the FSM

3) The resource library that is an input to the HLS process could contain what information? *1 point*

- [ ] Scheduling algorithm
- [ ] Component area
- [ ] Register allocation algorithm
- [ ] Component delay

No, the answer is incorrect.
Score: 0
Accepted Answers:
Component area
Component delay

4) If the output of an operation produced in one clock cycle is needed in a different clock cycle, which of the following are inferred? *1 point*

- [ ] A multiplexer
- [ ] A register
- [ ] An ALU
- [ ] An adder

No, the answer is incorrect.
Score: 0
Accepted Answers:
A register

5) Sharing of an adder by two different operations ALWAYS leads to the inference of a multiplexer at its input *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
FALSE

6) The numbers of registers inferred when a DFG is subjected to HLS is less than or equal to the number of DFG edges persisting across clock cycle boundaries *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

7) Pareto curve consists of those solution points that are: *1 point*

- [ ] The set of feasible solutions
- [ ] The set of infeasible solutions
- [ ] Not superior to any other point in the design space
- [ ] Not inferior to any other point in the design space

No, the answer is incorrect.
Score: 0
Accepted Answers:
Not inferior to any other point in the design space

8) The output of the lexical analysis phase consists of a stream of tokens *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

9) Verifying the grammar of the specification is the job of the Parser *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

10) The abstract syntax tree is usually created at the end of parsing a specification *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

11) Which of the following is NOT a valid information captured within resource library used in HLS? *1 point*

- [ ] Area of each component
- [ ] Functionality of each component
- [ ] Connections between different library components
- [ ] Delay of each component

No, the answer is incorrect.
Score: 0
Accepted Answers:
Connections between different library components

12) In high level synthesis, "type" mismatches in signal assignments present in the behavioral specification are checked during semantic checking *1 point*

- ( ) TRUE
- ( ) FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE