Unit 5 - Week 3

Assignment 3

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-08-21, 23:59 IST.

1) A simple 2-input AND gate can be modelled in VHDL with a process with no sensitivity list but with WAIT statements *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

2) A VHDL process having the statement "A<= B + C;" within it is always triggered when either B or C changes (assuming A, B, and C are signals) *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
FALSE

3) A WAIT statement of VHDL can occur within a loop. *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

4) A WAIT statement of VHDL CANNOT occur within a branch of an IF statement. *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
FALSE

5) One way of modelling combinational logic in a VHDL process is to place all the input signals in the sensitivity list *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

6) What does the following VHDL statement represent? "wait until X'event and X='1';" *1 point*

- An unconditional wait
- Signal X being 0
- Change in value of signal X
- A rising edge of signal X

No, the answer is incorrect.
Score: 0
Accepted Answers:
A rising edge of signal X

7) The purpose of a VHDL testbench could include which of the following applications? *1 point*

- To provide inputs to the design under test
- To observe outputs from the design under test
- To specify constraints for synthesis
- To report timing violations during simulation

No, the answer is incorrect.
Score: 0
Accepted Answers:
To provide inputs to the design under test
To observe outputs from the design under test
To report timing violations during simulation

8) Which of the following are realistic connections involving VHDL testbenches? *1 point*

- Output ports of the testbench are connected to the input ports of the design under test
- Input ports of the testbench are connected to the Input ports of the design under test
- The testbench is not connected to the design under test
- Input ports of the testbench are connected to the output ports of the design under test

No, the answer is incorrect.
Score: 0
Accepted Answers:
Output ports of the testbench are connected to the input ports of the design under test
Input ports of the testbench are connected to the output ports of the design under test

9) Generic parameters can be used in VHDL to parameterise: *1 point*

- Delays in signal assignments
- Widths of buses
- Names of entities
- Names of ports

No, the answer is incorrect.
Score: 0
Accepted Answers:
Delays in signal assignments
Widths of buses

10) VHDL processes can be nested (one process inside another process). *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
FALSE

11) VHDL variables are declared only within processes *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

12) VHDL signals are declared either within processes or within architectures *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
FALSE

13) In VHDL, the architecture to use for a specific entity can be specified using: *1 point*

- Generic clause
- Configuration statement
- wait statement
- Cannot be specified

No, the answer is incorrect.
Score: 0
Accepted Answers:
Configuration statement