Unit 3 - Week 1

Assignment 1

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-08-14, 23:59 IST.

1) In an Behavioural Level specification the decision of which operation to perform in which clock cycle, has not been taken yet *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
TRUE

2) In a Behavioural specification the external interface of a design is not indicated *1 point*

- TRUE
- FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
FALSE

3) What is an essential difference between the Chip design and Software design flows? *1 point*

- The chip design flow starts with a high level specification
- The chip design flow is subject to manufacturing errors
- The chip design flow is highly automated
- Formal verification is applicable to the chip design flow

No, the answer is incorrect.
Score: 0
Accepted Answers:
The chip design flow is subject to manufacturing errors

4) Design verification could be performed by checking equivalence between: *1 point*

- Behavioural and RTL level specifications
- RTL and Gate level specifications
- Gate level and optimised Gate level specifications
- Gate level specification and transistor level implementation

No, the answer is incorrect.
Score: 0
Accepted Answers:
Behavioural and RTL level specifications
RTL and Gate level specifications
Gate level and optimised Gate level specifications
Gate level specification and transistor level implementation

5) Which of the following is lowest in level of abstraction? *1 point*

- Adders
- Multiplexers
- Memory
- AND gate

No, the answer is incorrect.
Score: 0
Accepted Answers:
AND gate

6) Which of the following are true about the external interface of a simple memory module? *1 point*

- Address is a compulsory input
- Address is an optional input
- Address is a compulsory output
- Address is an optional output

No, the answer is incorrect.
Score: 0
Accepted Answers:
Address is a compulsory input

7) A netlist consists of what elements? *1 point*

- Component instantiations
- Interconnections
- Behavioural constructs
- Assignment statements

No, the answer is incorrect.
Score: 0
Accepted Answers:
Component instantiations
Interconnections

8) Automation is essential in the synthesis process for what reason? *1 point*

- The process can be applied to large specifications
- A single cell needs to be replicated a large number of times
- The hardware can be generated fast
- Computation in high-end processors needs to proceed at very high speed

No, the answer is incorrect.
Score: 0
Accepted Answers:
The process can be applied to large specifications
The hardware can be generated fast

9) When a netlist has a large number of gates, in what order are the components activated in the real hardware? *1 point*

- In increasing order of their sizes
- In decreasing order of their sizes
- In parallel
- In increasing order of their fanout

No, the answer is incorrect.
Score: 0
Accepted Answers:
In parallel

10) Which of the following steps belong to the 'Design' stage of the Chip design flow *1 point*

- Specification
- Slicing of a wafer
- Simulation
- Synthesis

No, the answer is incorrect.
Score: 0
Accepted Answers:
Specification
Simulation
Synthesis