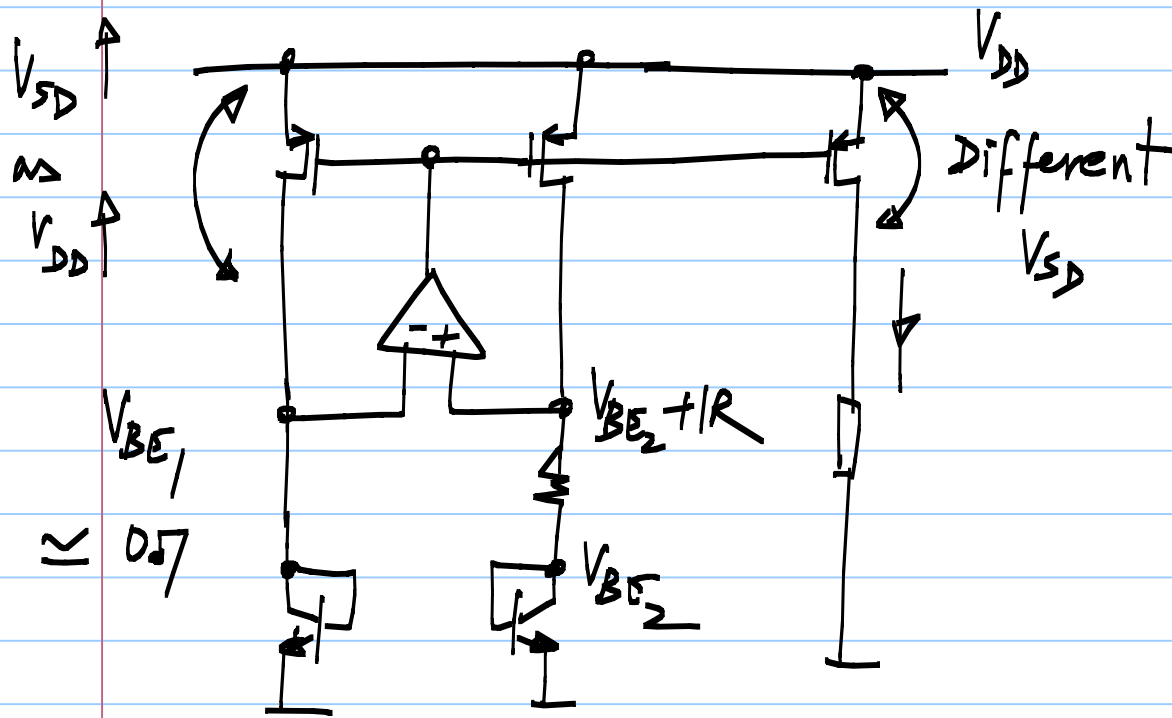
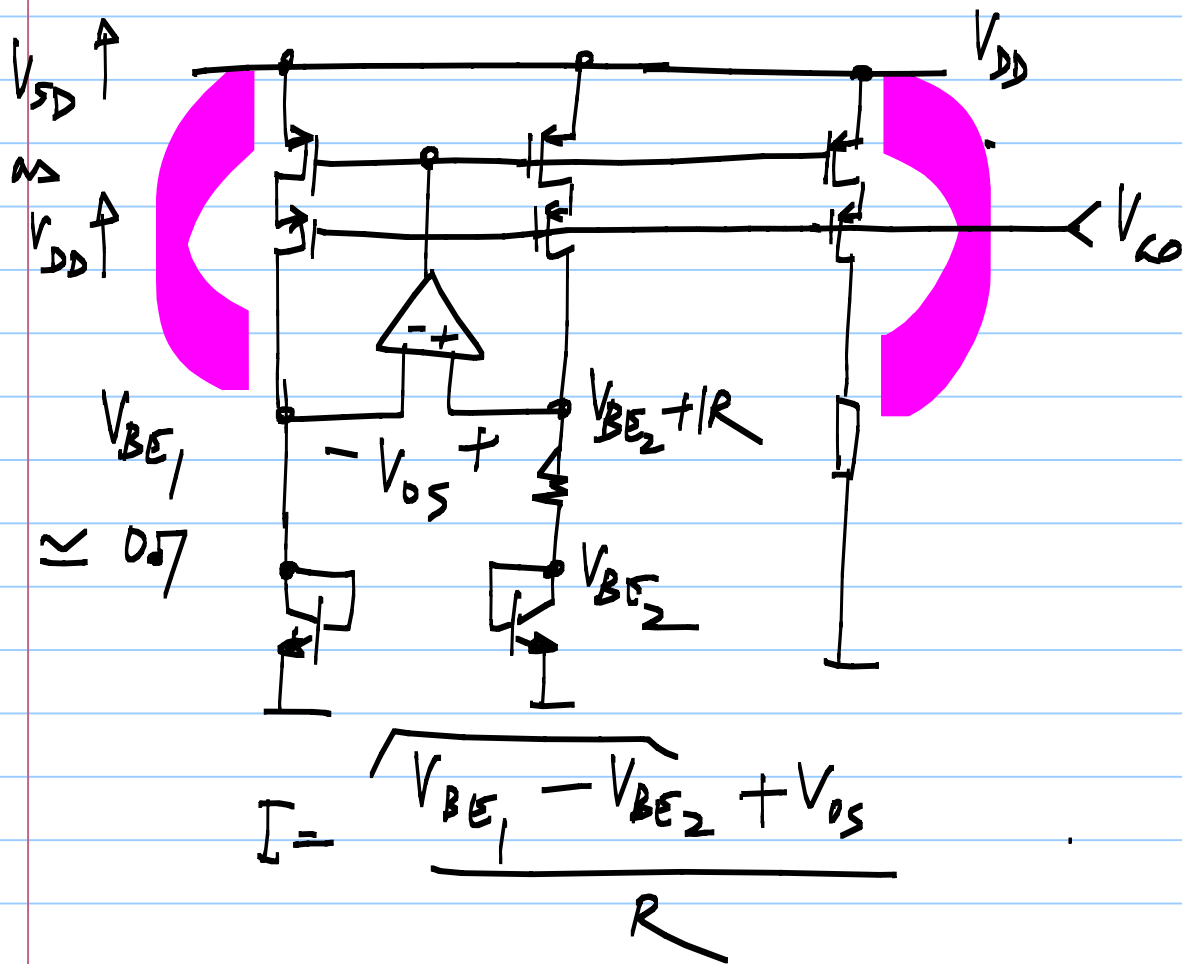


Lecture 54:

PTAT cell:





Sources of error

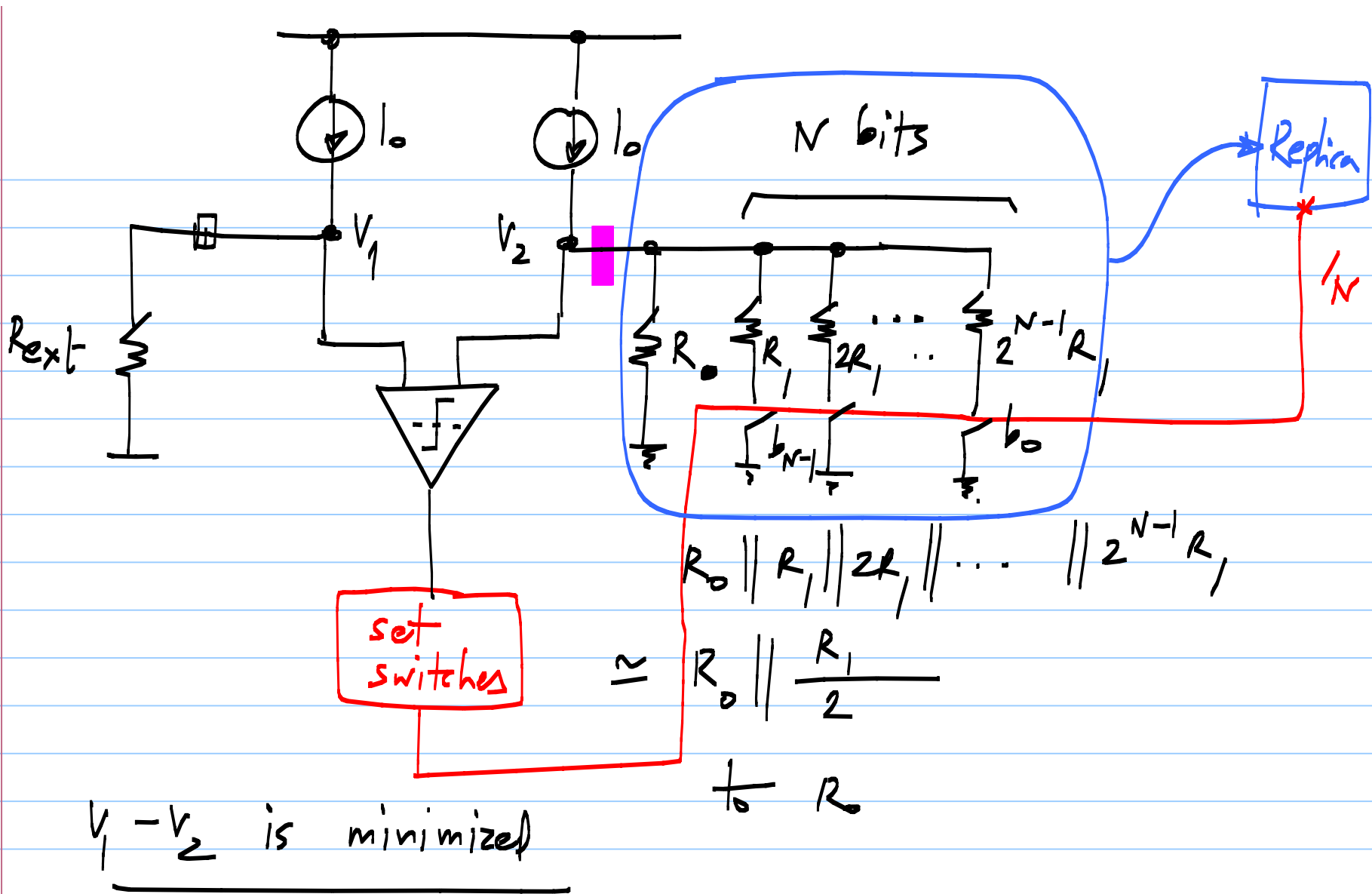
- * channel length mod. of PMOS
- Cascode
- * opamp offset
- Use large devices in the input pair

R : small TC

: constant with process variations

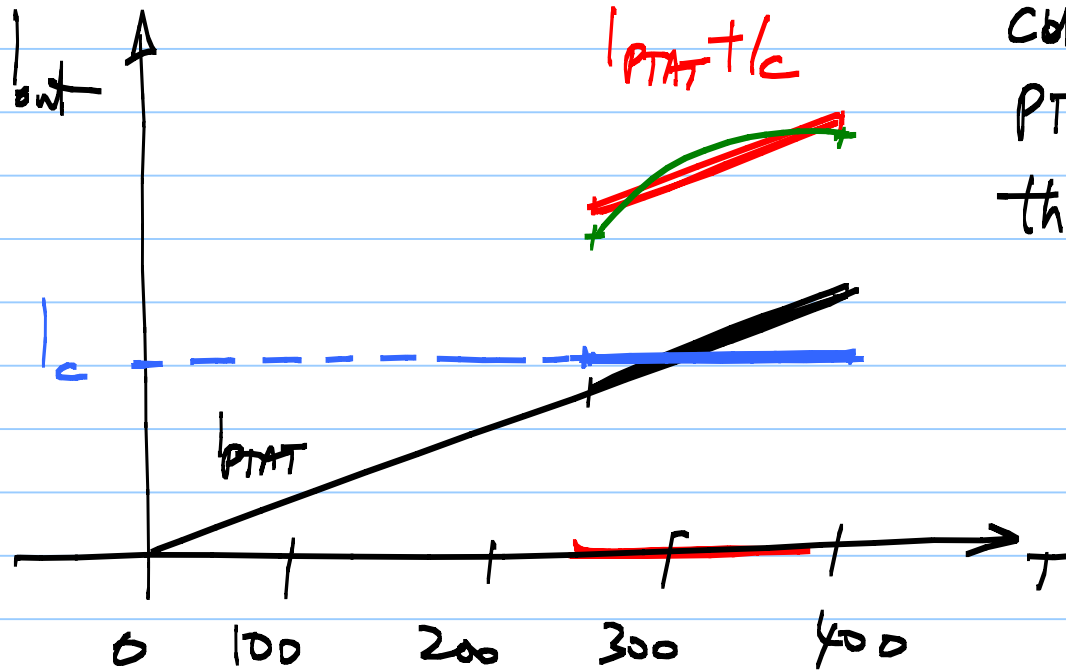
* External resistor.

* Single external resistor - Trim an internal resistor to that value



To generate currents with arbitrary dependence on temperature

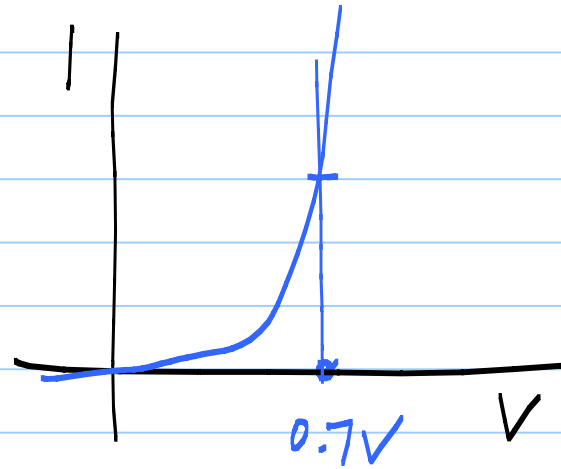
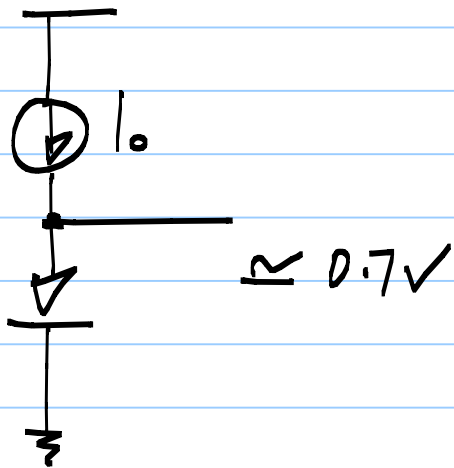
PTAT



Combine a constant current source & a PTAT current source in the right proportion

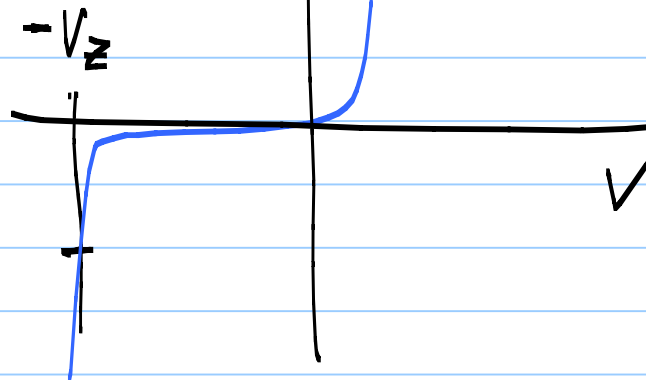
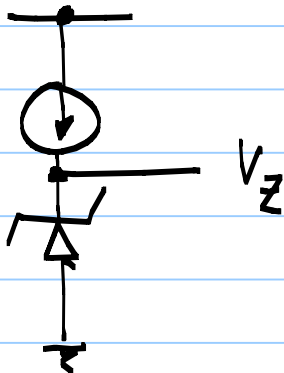
Constant voltage reference:

*



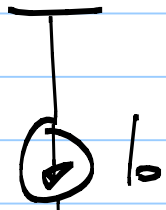
*

Zener diode



* Zener diodes around $V_Z = 3.6V$ have low temperature coefficient

Diode biased at a constant current:



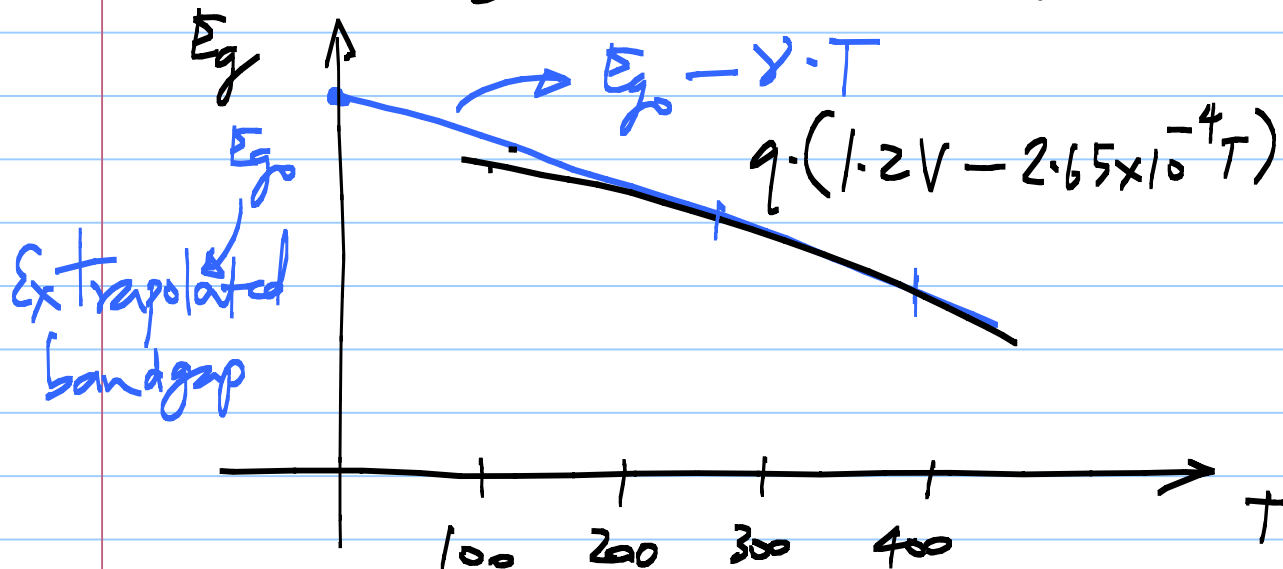
$$V_D = V_t \ln\left(\frac{I_0}{I_s}\right) = \frac{kT}{q} \ln\left(\frac{I_0}{I_s}\right)$$

$$I_s = b \cdot T^{4+m} \exp\left(-\frac{E_g}{kT}\right) \propto \underbrace{\mu \cdot kT \cdot n_i^2}_{(M_0 T^m)} \cdot \underbrace{T^3 \exp\left(-\frac{E_g}{kT}\right)}_{\text{Bandgap}}$$

$$m \approx -\frac{3}{2}$$

$$V_D = V_T \ln \frac{I_0}{b \cdot T^{4+m} \cdot \exp\left(-\frac{E_g}{kT}\right)}$$

$$= \frac{E_g}{q} + V_T \left[\ln\left(\frac{I_0}{b}\right) - (4+m) \ln(T) \right]$$



$$V_D = \frac{E_{g0}}{q} - 3.08 V_t + V_t \left[\ln\left(\frac{I_0}{I_b}\right) - (4+m) \ln(T) \right]$$

$$\frac{E_{g0}}{q} = 1.2V - 2.65 \times 10^{-4} T$$

$$= 1.2V - 3.08 V_t$$

$$V_D = \frac{E_{g0}}{q} + V_t \left[\ln\left(\frac{I_0}{I_b}\right) - 3.08 - (4+m) \ln(T) \right]$$

$$\approx 0.7V \quad 1.2V \quad \underbrace{\hspace{15em}}_{\substack{\text{Negative Voltage;} \\ \approx -0.5V}} \quad \underline{\text{Negative TC}}$$

Bandgap reference:

* Diode (V_{BE}) drop has a negative temp. coefficient of $\approx -1.5\text{mV/K}$

* Add a PTAT voltage to realize zero TC.

$$\begin{aligned} V_{out} &= V_D + \alpha \cdot V_T \\ &= \frac{E_{g0}}{2} + \underbrace{V_T \left[\ln\left(\frac{I_0}{b}\right) - 3.08 - (4+m)\ln T \right]}_{\text{set to zero at } 300\text{K}} + \alpha V_T \end{aligned}$$

$$\frac{dV_{out}}{dT} = \frac{k}{q} \left[\ln\left(\frac{I_0}{I}\right) - 3.08 - (4+m) \ln T \right] - \frac{kT}{q} \frac{(4+m)}{T} + \alpha \cdot \frac{k}{q} = 0$$

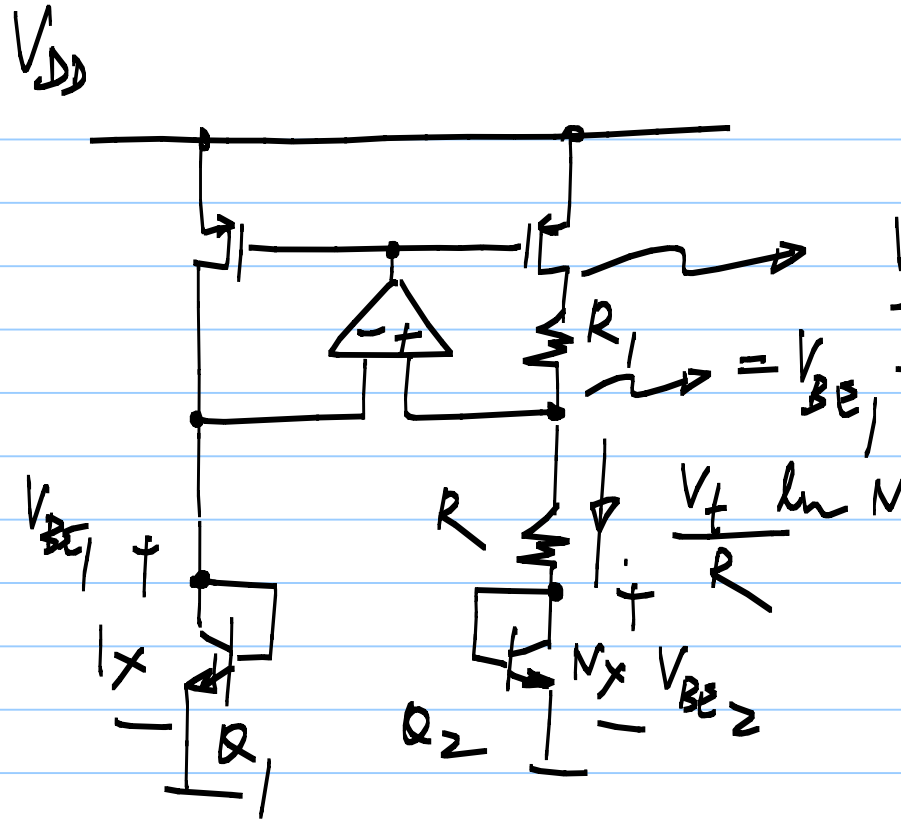
$$\alpha = - \left[\ln\left(\frac{I_0}{I}\right) - 3.08 - (4+m) \ln T \right] + (4+m)$$

$$= - \frac{V_D - E_{g0}/q}{V_t} + (4+m)$$

$$= \frac{E_{g0}/q - V_D}{V_t} + (4+m) \quad \begin{array}{l} \frac{500\text{mV}}{25\text{mV}} + 2.5 = \underline{\underline{22.5}} \\ \underline{\underline{21.5}} \end{array}$$

$$\begin{array}{l} E_{g0}/q = 1.2\text{V} \\ V_D = 0.7\text{V} \\ V_t = 25\text{mV} \\ m = -\frac{3}{2} \end{array}$$

PTAT cell



$$V_{BE1}$$

$$V_D + V_t \cdot \alpha$$

$$V_D + V_t \cdot \frac{R_1}{R} \cdot \ln(N)$$

$$\text{Set } \frac{R_1}{R} \ln(N) = \alpha$$

Currents are PTAT

$$I_c = I_0 \cdot \frac{T}{T_0}$$

$$V_b = V_T \ln \left(\frac{I_c}{I_s} \right)$$

$$= \frac{m E_g}{q} + V_T \left[\ln \left(\frac{I_0}{b} \right) - 3.08 - (4+m) \ln T \right]$$

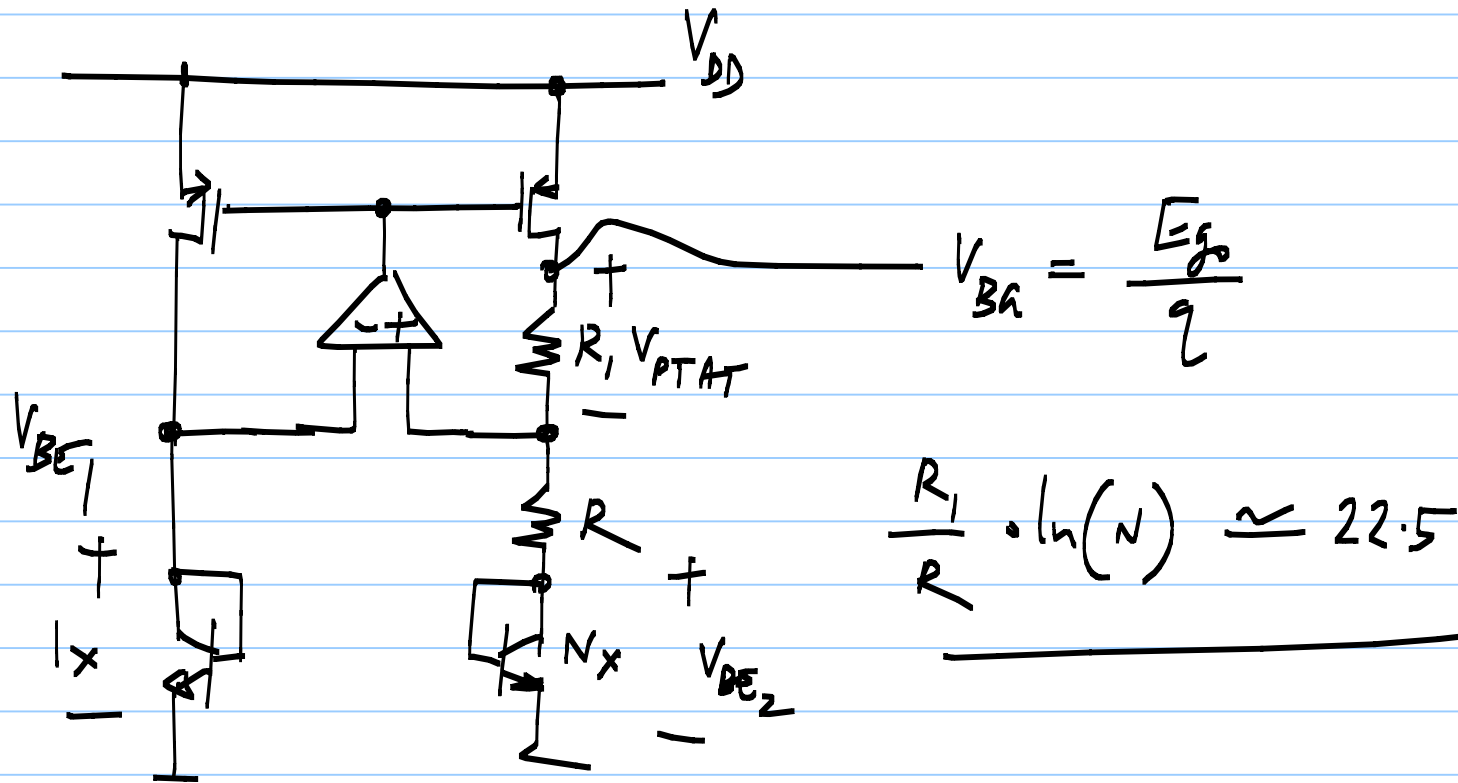
$$I_0 = I_0' \cdot \frac{T}{T_0}$$

$$\ln \left(\frac{I_0'}{T_0 b} \right) + \ln T$$

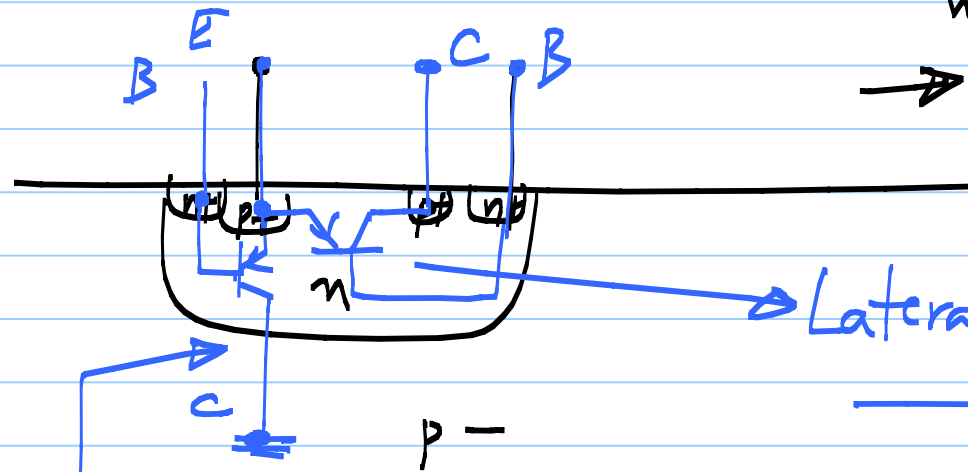
PTAT

$$\frac{E_g}{q} + V_T \left[\ln \left(\frac{I_0'}{T_0 b} \right) - 3.08 - (3+m) \ln T \right]$$

Bandgap voltage reference:



In a CMOS process:



Lateral PNP

Substrate PNP



Matching

$$\frac{Q_1 : Q_2}{1 : 8}$$

Offset

[Large devices]

