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Analog Circuits can be implemented on two Technologies :

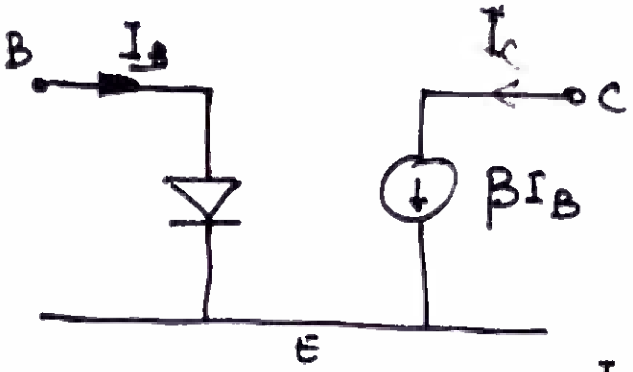
1. Bipolar

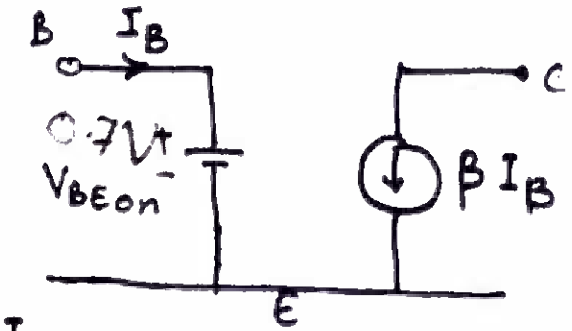
2 MOS

Both have certain Advantages and Disadvantages However as 'Most' of Silicon ICs are Digital Systems, the major technology is MOS Technology Hence Analog Blocks need to be designed for MOS Tech.

Large Signal Model

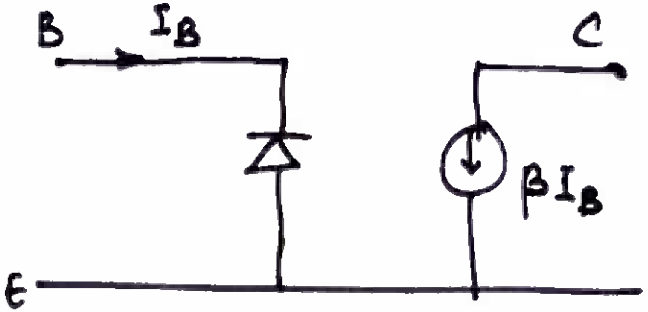
Case of Common Emitter Configuration

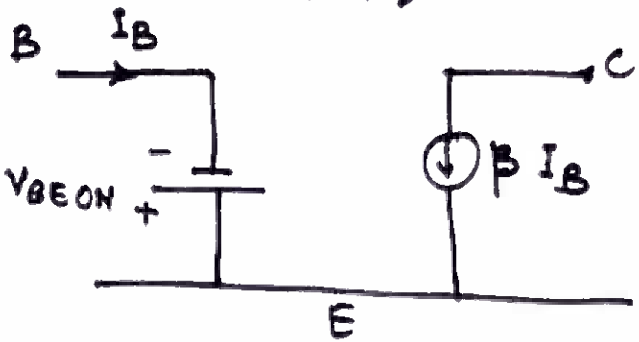




(npn)

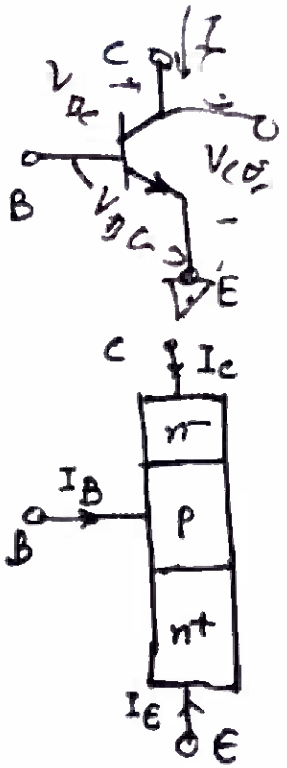
$$I_B = \frac{I_S}{\beta} \exp\left(V_{BE}/V_T\right)$$





(pnp)

Bipolar Transistor Models



$$I_E = I_B + I_C \quad \text{(Universal)} \qquad -(1)$$

$$I_C = \alpha I_E \qquad \alpha = \alpha_T \gamma \qquad -(2)$$

$$\frac{I_C}{I_B} = \beta \qquad \therefore \quad \beta = \frac{\alpha}{1-\alpha} \qquad -(3)$$

β is called Forward Current Gain

$$I_C = \alpha I_E + I_{CO} \qquad -(4)$$

$$I_{CO} = I_{CS}(1 - \alpha_F \alpha_R) \qquad -(5)$$

$$V_{CE} = V_{BE} + V_{BC} \qquad -(6)$$

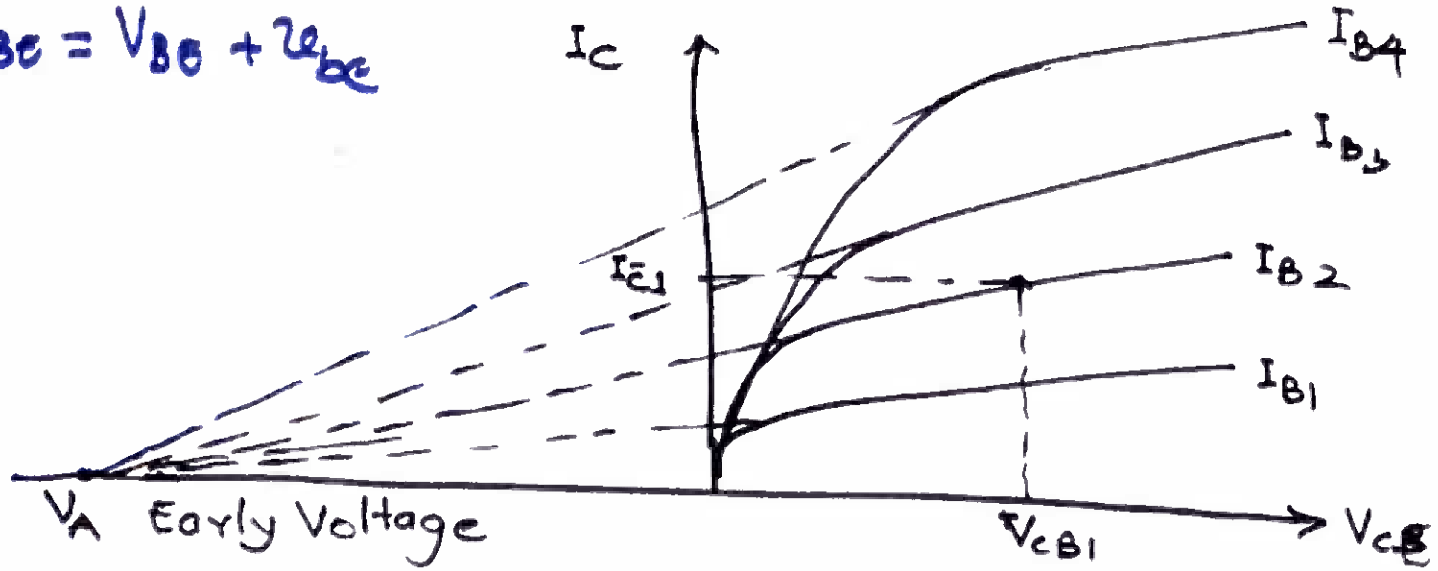
Small-Signal Model of BJT

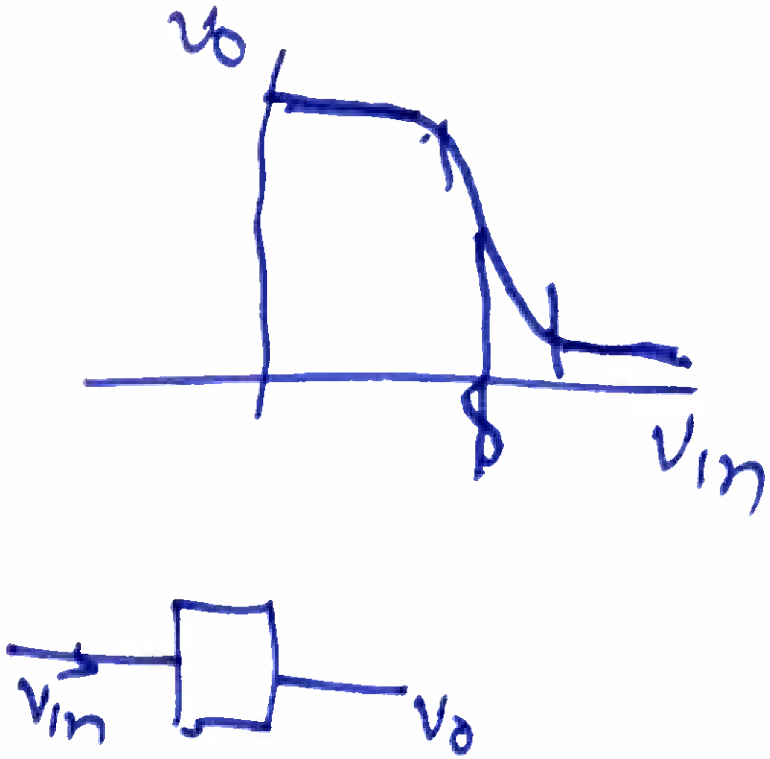
$$I_b = i_b + I_B$$

Total = Small Signal + DC

$$I_C = i_c + I_C$$

$v_{BE} = V_{BE} + v_{be}$





Small Signal Model (Cont.)

Most Important parameter of Transistor is

Transconductance $g_m = \dfrac{\partial I_c}{\partial V_{BE}}$ — (1)

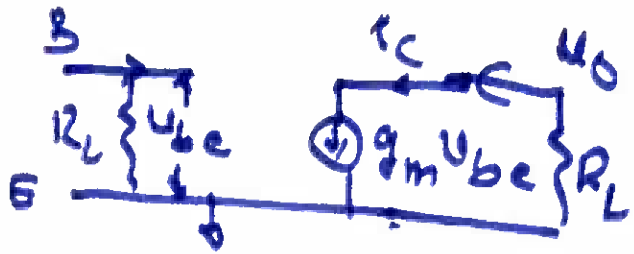
$(I_c = I_s \exp(V_{BE}/V_T)$

We have

$$\Delta I_c = \frac{dI_c}{dV_{BE}} \cdot \Delta V_{BE}$$

OR $\Delta I_c = g_m \Delta V_{BE}$

i.e. $i_c = g_m v_{be}$ — (2)



$v_o = -i_c R_L$

$v_o = -\beta_0 i_b R_L$

$i_b \cdot R_i = v_{be}$

$\dfrac{v_o}{v_{be}} = -\dfrac{\beta_0 R_L}{R_i}$

We have $I_C = I_S \exp(V_{BE}/V_T)$

$$\therefore g_m = \frac{d}{dV_{BE}}\left[I_S \exp(V_{BE}/V_T)\right]$$

$$= \frac{I_S}{V_T} \text{Exp}(V_{BE}/V_T) = \frac{I_C}{V_T} = \frac{I_C}{(kT/q)} = \frac{qI_C}{kT}$$

$$\therefore g_m = \frac{qI_C}{kT} \quad - (3)$$

Typically at 27°C (Room Temp.) $\frac{kT}{q} \simeq 26$ mV

$\therefore$ at $I_C = 1$ mA (say) $g_m \simeq 38$ mA/V

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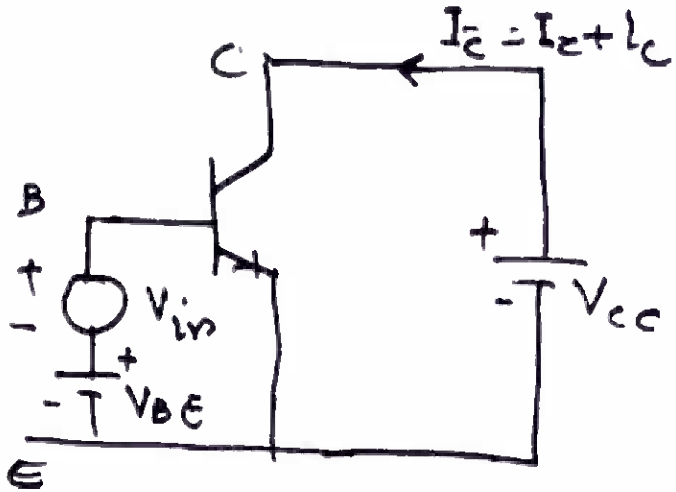
Small Signal Limitation

Example of CE Amplifier



$$I_c = I_S \exp\left[\frac{V_{BE} + V_{in}}{V_T}\right] \quad \text{Total}$$

&

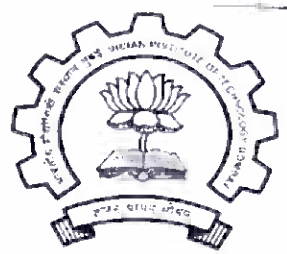
$$I_c = I_S \exp\left[\frac{V_{BE}}{V_T}\right] \quad \text{DC}$$

$$\therefore I_c = I_C \exp\left(V_{in} / V_T\right)$$

If $V_{in} < V_T$

$$I_c = I_C \left[1 + \frac{V_{in}}{V_T} + \frac{1}{2}\left(\frac{V_{in}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{in}}{V_T}\right)^3 + \cdots\right]$$

As $i_c = I_c - I_C$



Hence $i_c = \frac{I_C}{V_T} v_{in} + \frac{1}{2}\frac{I_C}{V_T^2} v_{in}^2 + \frac{1}{6}\frac{I_C}{V_T^3} v_{in}^3 \ldots\ldots$

If $v_{in} << V_T$ Then Higher Order terms are negligible

$\therefore i_c = \frac{I_C}{V_T} . v_{in}$ & then $g_m = \frac{i_c}{v_{in}} = \frac{I_C}{V_T} = \frac{qI_C}{kT}$

Hence for Small Signal operation

$$v_{in} << 26\,mV$$

BJT Model (cont.): Capacitance

If a small signal voltage V_{in} is applied over dc value V_{BE}, then we say

$$\Delta V_{BE} = V_{in} \quad \& \quad \Delta Q_e = q_e$$

and $$\Delta Q_b = q_b$$

Then small signal (ac) capacitance across BE jn is given by

$$C_{be} = \frac{q_b}{V_{in}}$$

From Transistor theory, we know minority charge in Base is $Q_e = I_c \tau_b$ where τ_B is called Base Transit time

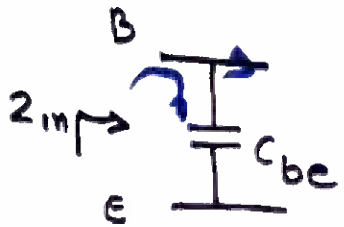
or $\Delta Q_e = \tau_B \Delta I_c$ From charge neutrality $\Delta Q_e = \Delta Q_b$

$\therefore \Delta Q_b = \Delta I_c \tau_B$

or $q_b = i_c \tau_B$ (small signal representation)

Therefore $C_{be} = \frac{i_c \tau_B}{v_{in}} = \left(\frac{i_c}{v_{in}}\right)\tau_B = g_m \tau_B$

$C_{be} = C_\pi' = \frac{q I_C}{kT} \cdot \tau_B$ $\left(\tau_B = \frac{W_B^2}{2 D_n} \text{ for npn}\right)$

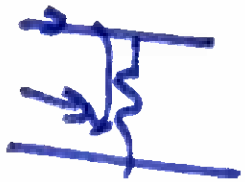


At Lower frequency $Z_{in} = \frac{1}{j\omega C_{be}}$ is large

as C_{be} is normally very small (<pf range)

$\therefore$ At low Frequency, this shunting Capacitance can be neglected.

Input resistance



We have $I_C = \beta I_B$

or $I_B = \frac{1}{\beta} I_C$

or $\Delta I_B = \frac{d}{dI_C}\left(\frac{I_C}{\beta}\right)\Delta I_C$

We define ac β as $\beta_0 = \frac{\Delta I_C}{\Delta I_B} = \frac{i_c}{i_b} = \left[\frac{d}{dI_C}\left(\frac{I_C}{\beta}\right)\right]^{-1}$

β_0 is called Small Signal current Gain

If β is constant, $\beta_0 = \beta_{dc}$ else β_0 is different from β.

Then, Input Resistance $r_\pi = \frac{v_{in}}{i_b} = \frac{v_{in}}{i_c} \cdot \beta_0 = \frac{\beta_0}{g_m}$

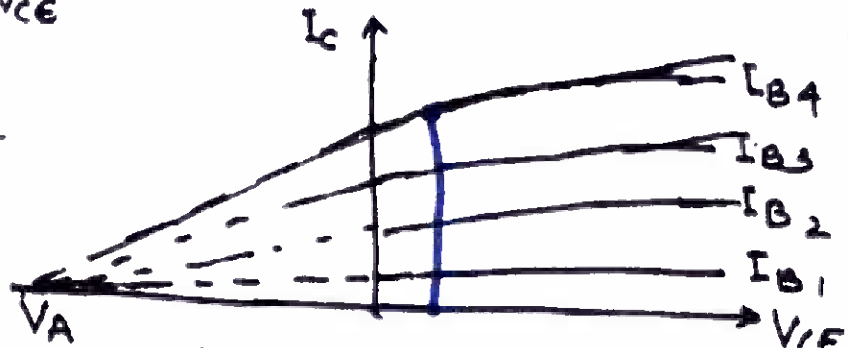
$\therefore \boxed{\beta_0 = g_m r_\pi}$ or $\frac{i_c}{i_b} = \left(\frac{kT}{qI_C}\right)^{-1} \cdot r_\pi = \frac{I_C}{I_B}$ $\therefore \boxed{r_\pi = \frac{kT}{qI_B}}$

Output Resistance

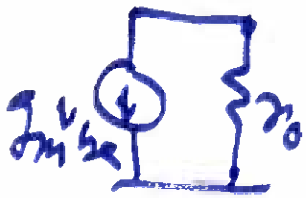
We have found earlier

$$\Delta I_c = \frac{\Delta I_c}{\Delta V_{CE}} \Delta V_{CE}$$

or $$\frac{\Delta V_{CE}}{\Delta I_c} = \frac{V_A}{I_c}$$



$\frac{\Delta V_{CE}}{\Delta I_c}$ is slope of I_c-V_{CE} characteristics



$\therefore$ Output Resistance $r_o = \frac{\Delta V_{CE}}{\Delta I_c} = \frac{v_{ce}}{i_c} = \frac{V_A}{I_c}$

where V_A is Early Voltage

We define a parameter η is

$$\eta = \frac{kT}{q} \cdot \frac{1}{V_A}$$

$$= \frac{kT}{qI_C} \cdot \frac{I_C}{V_A} = \frac{1}{g_m} \cdot \frac{1}{r_o}$$

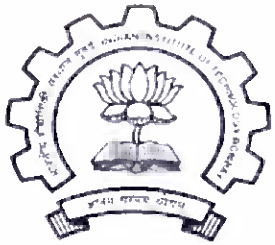
or $\boxed{g_m r_o = \frac{1}{\eta}}$

Typically V_A varies between 50 to 100 Volts

Further at $T = 300^0 k$, $\eta \simeq 2.6 \times 10^{-4}$ for above $V_A = 100V$

For operating current of $I_C = 1mA$, we get $r_o = \frac{100}{10^{-3}} = 100k\Omega$

Base-Emitter J^n Capacitance C_{je}



As we did evaluation for C_μ, we do the same for C_{je} which is BE J^n capacitance

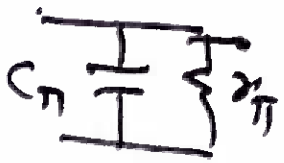
$$C'_{je} = \frac{C_{jeo}}{\left(1 - \frac{V_{BE}}{\phi_0}\right)^n}$$

. But this is not value which is valid.

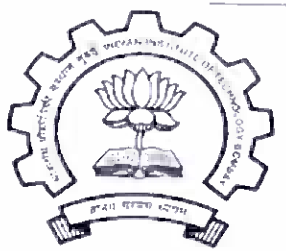
BE J^n is FB and hence this formulae is not correct

Typically we take $\boxed{C'_{je} = 2 \cdot C'_{jeo}}$

Then Input capacitance $\boxed{C_\pi = C_{be} + C'_{je}}$



Base-Collector Jn Capacitance C_μ



C_μ => Varies with variation in V_{CB} as junction is in Reversed-Biased State.

We know RB Jn capacitance of a diode (with Step Jn) is given by

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^{1/2}}$$

($1/2$ may become $1/3$ for linearly Graded junction)

ϕ_0 = Built-in Potential $= \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$

Hence in Transistor

$$C_\mu = C_{\mu 0} / \left(1 - \frac{V_{CB}}{\phi_0}\right)^n \qquad (n = 1/2 \text{ or } 1/3)$$

Collector - Base resistance r_μ

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As V_{BE} gets modulated due to V_{in}, the Base-Collector junction bias too get modulated That V_{CB} changes due to change in I_B

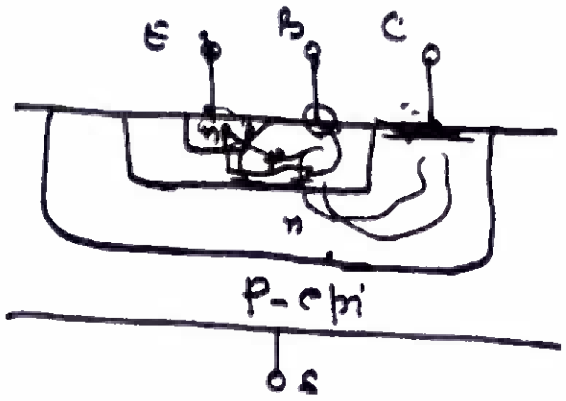
We define

$$r_\mu = \frac{\Delta V_{CB}}{\Delta I_B} = \frac{\Delta V_{CE}}{\Delta I_C} \cdot \frac{\Delta I_C}{\Delta I_B} = \frac{v_{ce}}{i_c} \cdot \frac{i_c}{i_b}$$

$$\therefore \boxed{r_\mu = r_o \cdot \beta_o}$$

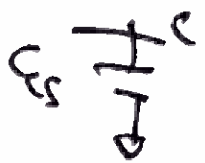
This resistance is between Base & C J' Base and Collector regions.

Collector Substrate Capacitance C_{cs}



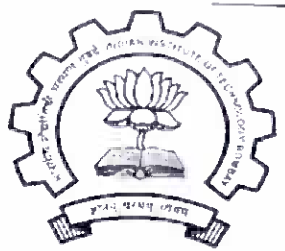
Since in an IC, collector is a diffused region in substrate, one observes presence of a collector - substrate junction with capacitance

$$C'_{js} = \frac{C'_{cso}}{\left(1 - \frac{V_{cs}}{\phi'_0}\right)^n}$$



Normally substrate is Grounded. Hence C_{cs} is the collector capacitance between Collector terminal & Ground

Parasitic Resistances $r_{bb'}$, r_{eb} & r_c



1. $r_{bb'}$:– Base Resistance

2. r_{es} :– Emitter Region Resistance

3. r_c :– Collector Region Resistance.

Using these parameters we can now Create the Small Signal Equivalent Circuit of a Bipolar Transistor.

Equivalent Circuit of BJT