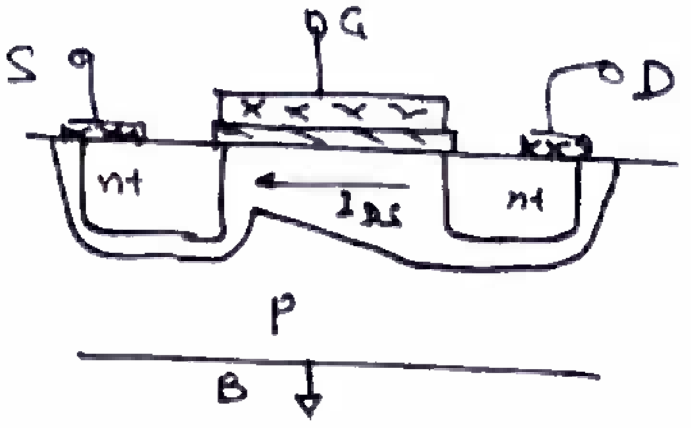
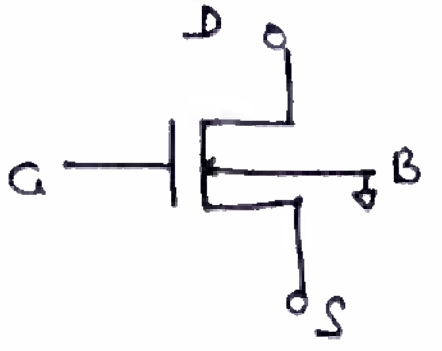
MOS Transistor – A Circuit View of a Device



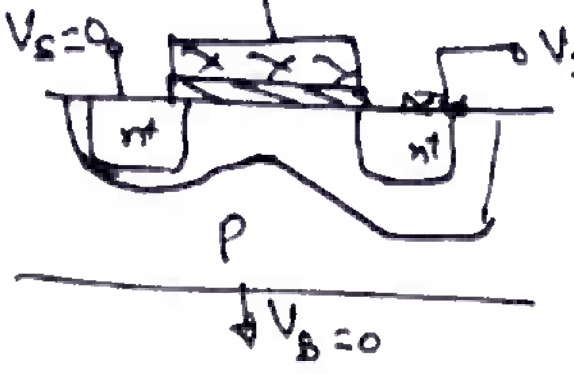


Case I : $V_G = V_S = V_D = V_B =$ 0 Volt,

We observe $I_{DS} = 0$. Which means Transistor is 'OFF'

In Current Technology Node (Say Less than 90 nm) too, This is Valid as Ohms Law cannot be violated

Case 2. $V_{GS}=0$



$V_S = 0$

$V_{GS} = V_{BS} = 0$

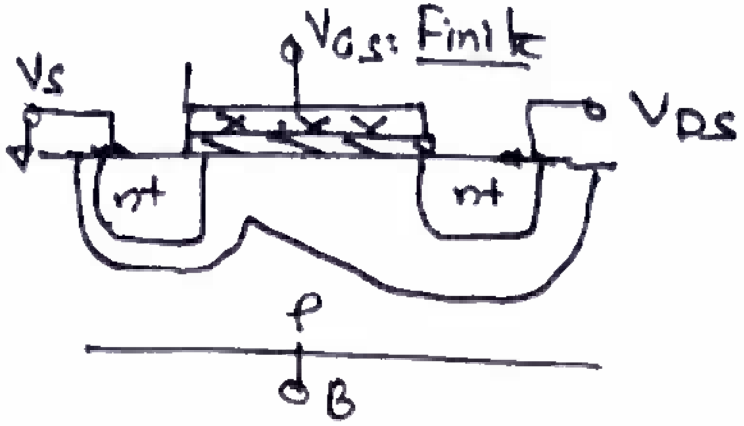
But V_{DS} => Positive (>0)

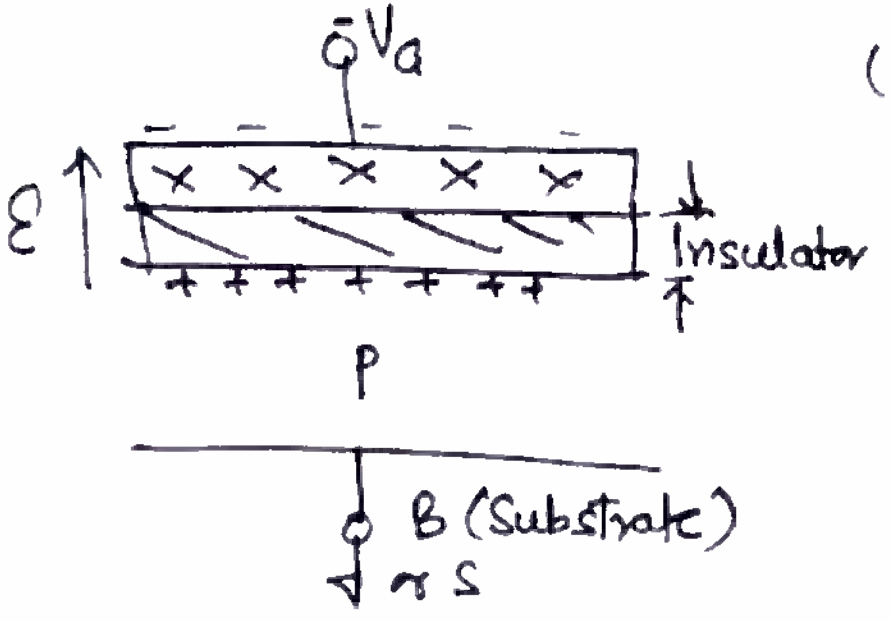
$I_{DS} = 0$ in Ideal Condition

as Both the Diodes Source/Bulk & Drain/Bulk are Reverse Biased

However in newer technologies due to reduced dimensions and increased doping in channel area, One observes I_{DS} is not negligible. Transistor is Partially 'ON' (Problem Case)

Case 3





Holes accumulate near Interface

V_{GS} is Finite

$V_{DS} = 0$, $V_{BS} = 0$

This Is equivalent case of MOS capacitor

(i) $V_{GS} < 0$ (-ve) Accumulation Mode

Gate gets -ve charge ($+Q_m$)

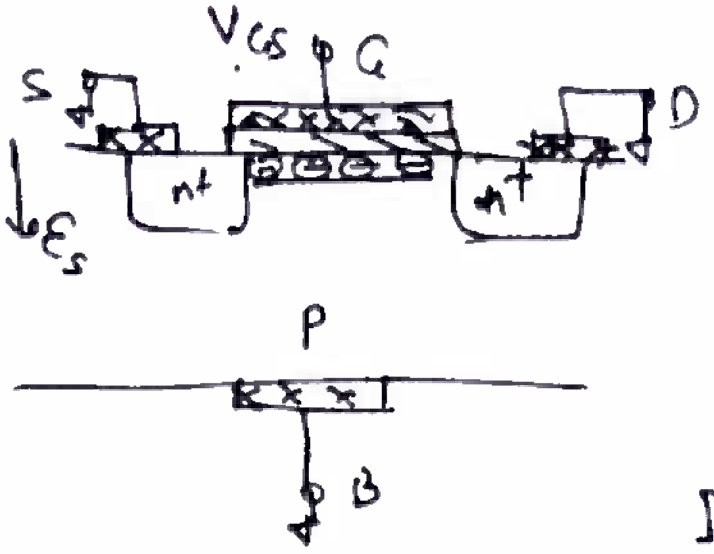
Due to Gausse's Law Semiconducter Surface beloco the dielectric layer, must produce equivalent + charge Q_s , Such that $Q_m + Q_s = 0$

As Q_m = -ve

$\therefore Q_s$ is Positre

Assumption $Q_{ox} = 0$

(ii) V_{GS} Positive & Small.



Hence 'Gate' Plate gets a charge $+Q_m$.

By Gausse's Law

Now Q_s is $-ve$

In P-Semiconductor $-ve$ Q_s can be obtained by holes getting depleted at the Interface Leaving $-ve$ly charged Depletion layer due to Ionised Acceptors $(-qN_a^-)$. This mode is called Depletion Mode.

Additional -ve charge is provided by free electrons at the Interface. This layer of free electrons (-ve charge) is opposite that of substrate giving +ive charges due to Holes. Hence this layer is called Inversion layer (n-layer).

$$V_{GS} = V_T = 2\phi_F - \frac{Q_S}{C_{ox}} = 2\phi_F + \frac{\sqrt{2\varepsilon N_a \bar{} x_{dmax}}}{C_{ox}}$$

Both terms on RHS are now Positive

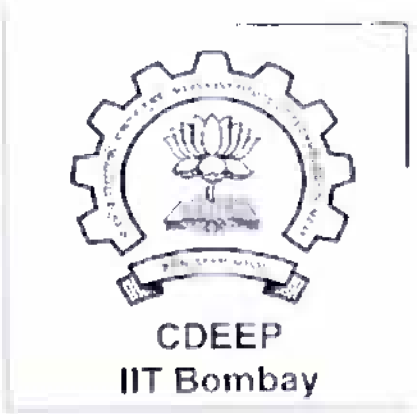
$\therefore$ V_T for n-channel device is Positive

Two Assumptions were made here

(i) $Q_{ox} = 0$ (ii) $\phi_{ms} = \phi_m - \phi_s = 0$

If we take these into account

$$V_T = \phi_{ms} + 2\phi_f - \frac{Q_{ox}}{C_{ox}} - \frac{Q_S}{C_{ox}}$$



$$\psi_s + V_{ox} = V_{gs}$$

V_{ox}

$D = \epsilon_s \mathcal{E}_s$

$\epsilon_s \mathcal{E}_s = \mathcal{E}_{ox} \epsilon_{ox}$

$Q_s = -\epsilon_s \mathcal{E}_s$

$$Q_m + Q_s + Q_{ox} = 0$$

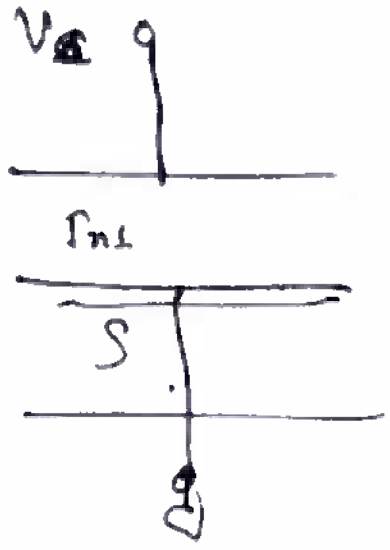
$\epsilon_s \mathcal{E}_s = \left(\frac{\epsilon_{ox}}{t_{ox}}\right) V_{ox}$

$Q_m = -(Q_s + Q_{ox})$ ← Q_s'

$-Q_s = C_{ox} V_{ox}$

$$V_{ox} = -\frac{Q_s}{C_{ox}}$$

$$V_T = 2\phi_F - \left.\frac{Q_s'}{C_{ox}}\right|_{V_{GS}=V_T} = 2\phi_B - \frac{-2N_a \bar{x}_{dmax}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

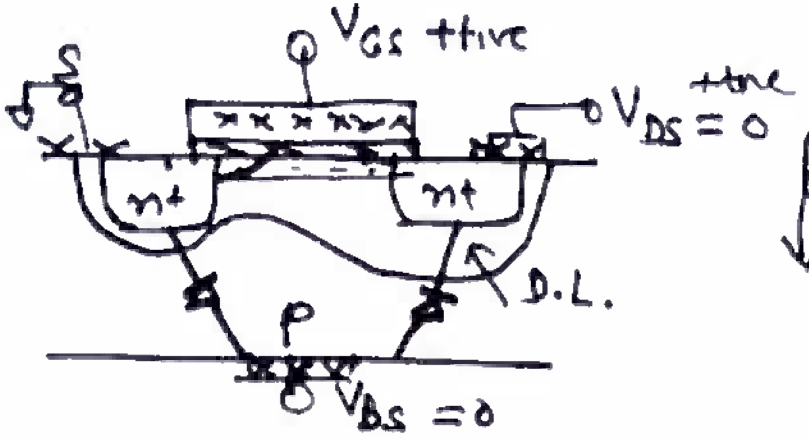


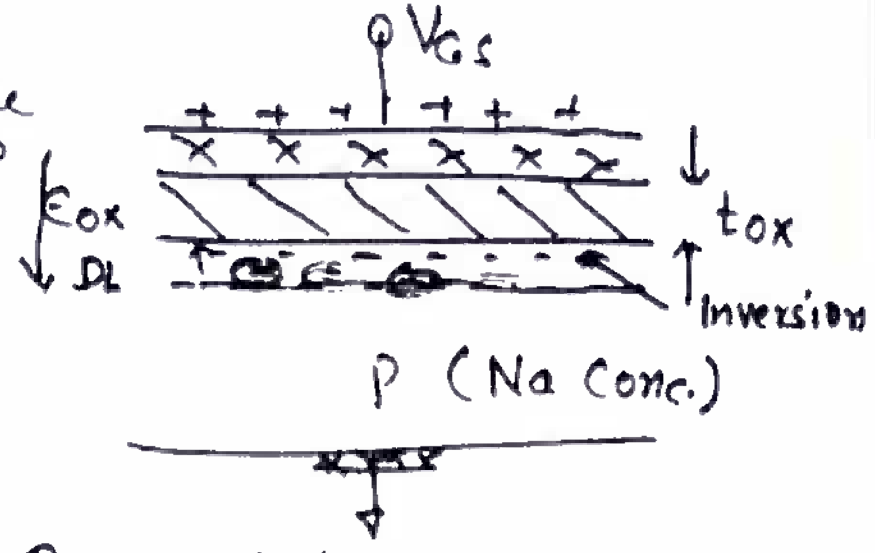
$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\epsilon}$$

$$V_G = V_{ox} + \psi_s \qquad \mathcal{E} = -\frac{dV}{dx}$$

$$Q_{n_{n_0}} \propto e^{q\psi_s/kT}$$

(iii) V_{GS} +tive and substantial





V_{GS} +tive makes Q_m substantially larger +tive

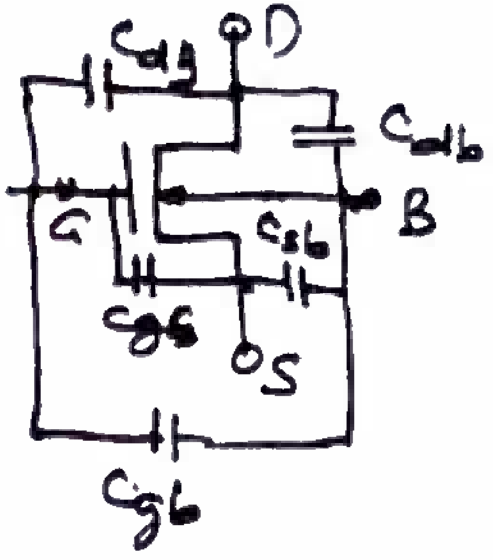
However at a value of $V_{GS} = V_T$, the Depletion layer thickness $x_d = \sqrt{\frac{2 k_s \epsilon_0}{q N_a} \psi_s}$ becomes maximum

at $\psi_s = 2\phi_F = \frac{2kT}{q} \ln \frac{N_a}{n_i}$ (2x Fermi Potential)

and Depletion Charge $Q_B = -qN_a x_{dmax}$ constant

If $V_{GS} \geq V_T$ then what is the Source -ve charge?

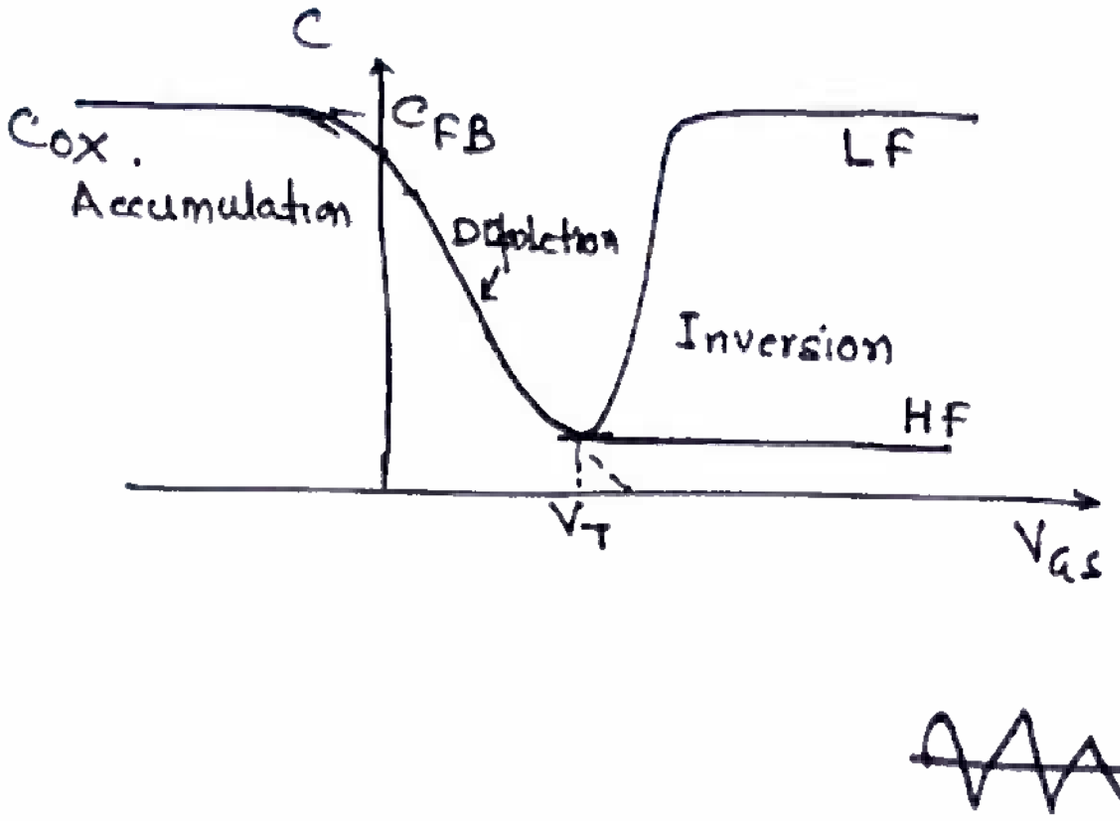
Intrinsic MOS Capacitor MODEL IN TRANSISTOR



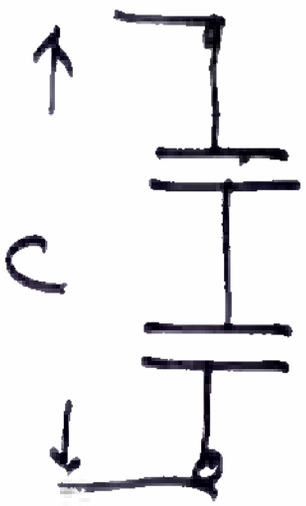
	Sub V_T	Linear	Saturated (Active)
C_{gs}	0	$\frac{1}{2} WL C_{ox}$	$\frac{2}{3} WL C_{ox}$
C_{gd}	0	$\frac{1}{2} WL C_{ox}$	0
C_{gb}	$\left(\frac{1}{2}\frac{\epsilon_s W \cdot L}{x_d} + \frac{1}{WLC_{ox}}\right)$	0	0

$C_{in} \simeq C_{gs} + C_{gb} + C_{gd} \simeq C_{ox}$ for all regions !!

C-V characteristics



$\epsilon_s = k_{Si} \cdot \epsilon_0$



$C_{S_{min}} = \frac{\epsilon_s}{x_{d_{max}}}$

Assumption 2 :—

$$\mathcal{E}(y) = \frac{V_{DS}}{L}$$

$v = \mu \mathcal{E}(y)$ is always true.

In reality $v \longrightarrow v_{sat}$

Assumption 3 :—

The I_{DS} current is wholly due to channel charge.

→ Only Drift Current occures.

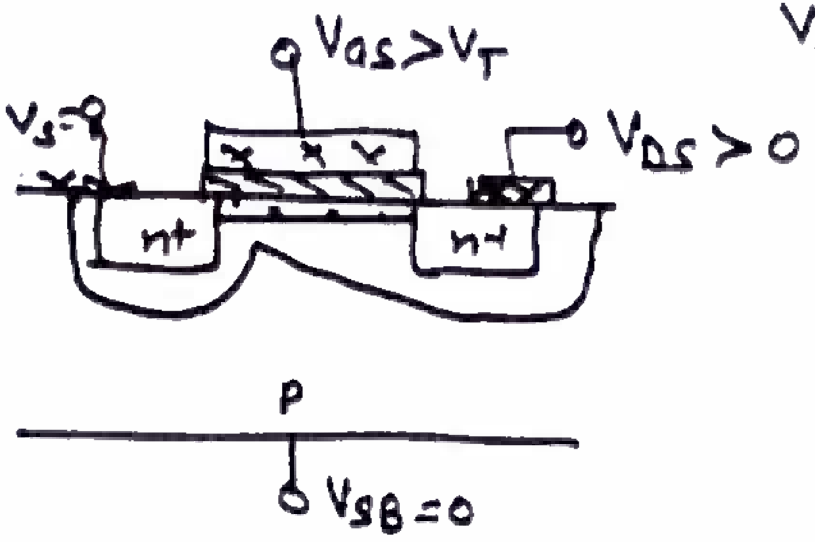
Though in very short channel devices in new Structures Diffusion currents may be contributing ?!

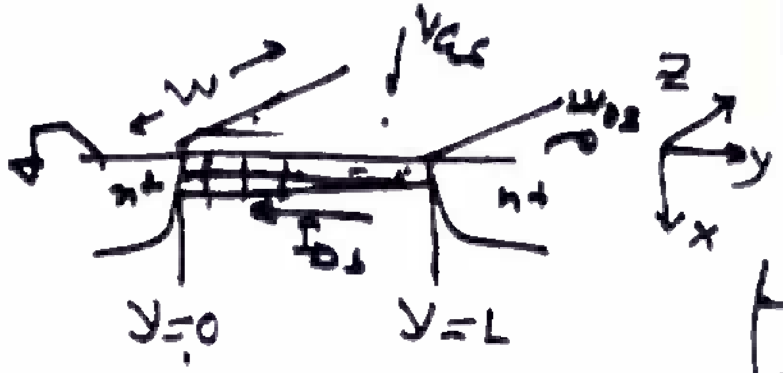
Assumption 4 :— Even in Assumption 2, we have μ constant ?

Case 4 :—

$V_{GS} > V_T$ $\quad V_{SB} = 0$

$V_{DS} > 0$ $\quad V_S = 0$





Assumption 1 :— Gradual Channel Approximation

$$\mathcal{E}(x) >> \mathcal{E}(y)$$

Channel charge is decided only by V_{GS}

or to say Inversion charge $Q_n(y) = C_{ox}(V_{GS} - V_T - V(y))$

And $I_{DS} = Q_n v \cdot W$; $\quad v = \mu \mathcal{E}(y)$

With these First Order Assumptions

$$I_{DS} = C_{ox}\left[V_{GS} - V_T - V(y)\right]\mu\,\mathcal{E}(y)\cdot W$$

as $$\mathcal{E}(y) = \frac{dV(y)}{dy}$$

$$I_{DS}\cdot dy = W\mu C_{ox}\left[(V_{GS}-V_T) - V(y)\right]dV(y)$$

$$I_{DS}\int_0^L dy = W\mu C_{ox}\int_0^{V_{DS}}\left[(V_{GS}-V_T) - V(y)\right]dV(y)$$

$$\text{or}\quad I_{DS} = \frac{\mu C_{ox}}{\uparrow \beta'}\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$\beta = \beta'\left(\frac{W}{L}\right)$

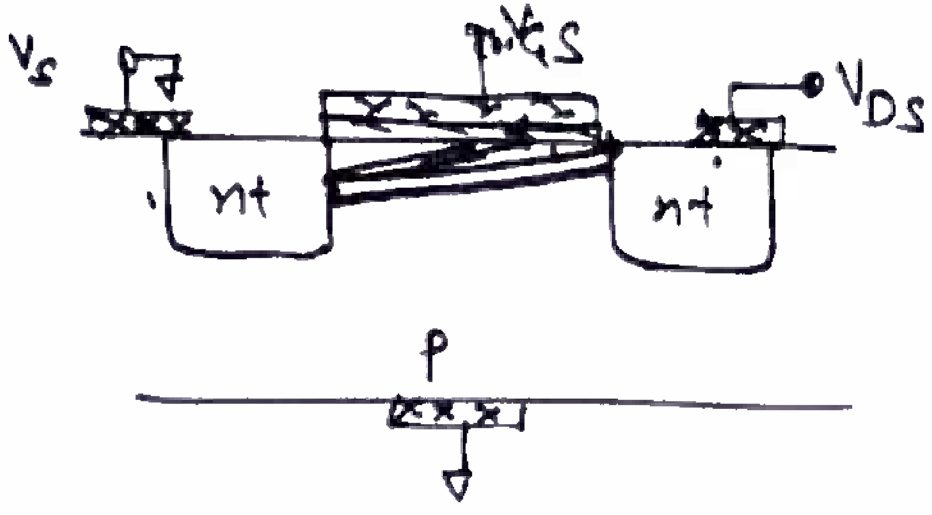
→ See Plot now ?

But that's not True as per Experiments.

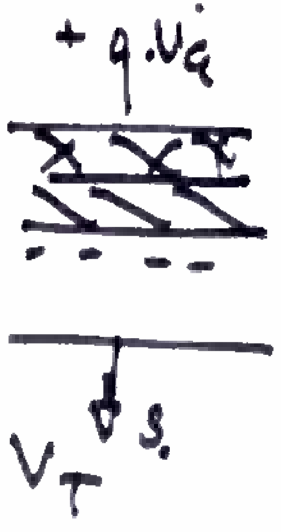
So what happens at

$$V_{GS} - V_T = V_{DS}$$

& beyond.

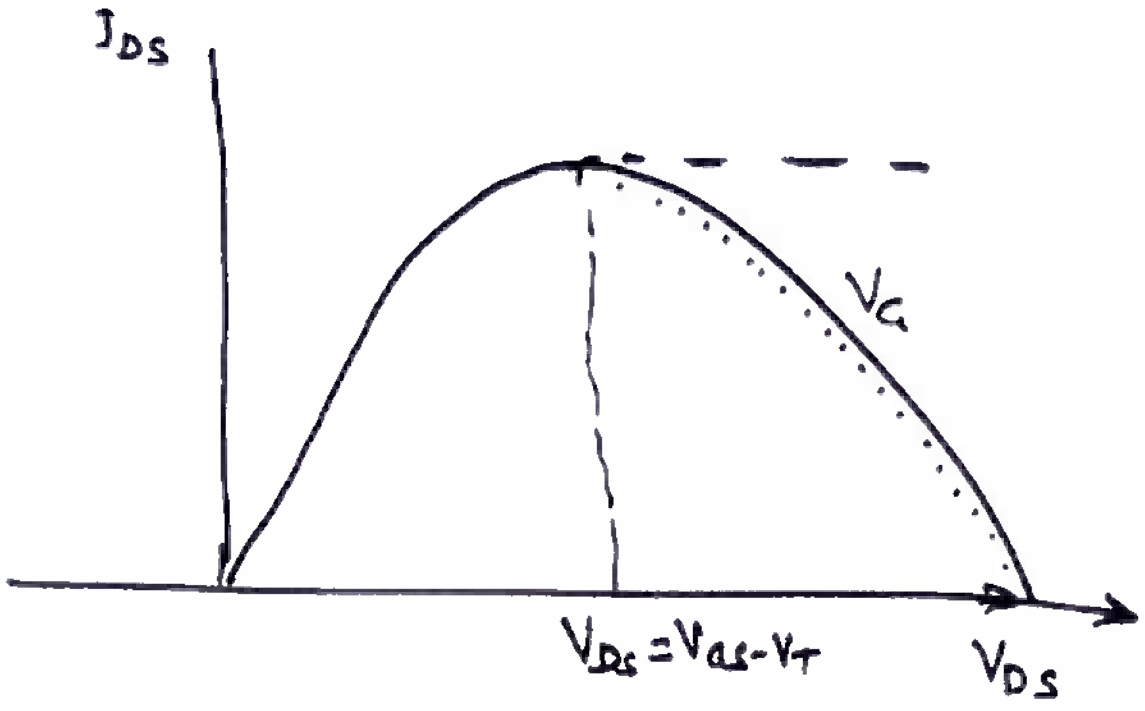


Saturation ?



$V_{GS} - V_{D_{sat}} = V_T$

$V_G - V_S \geq V_T$

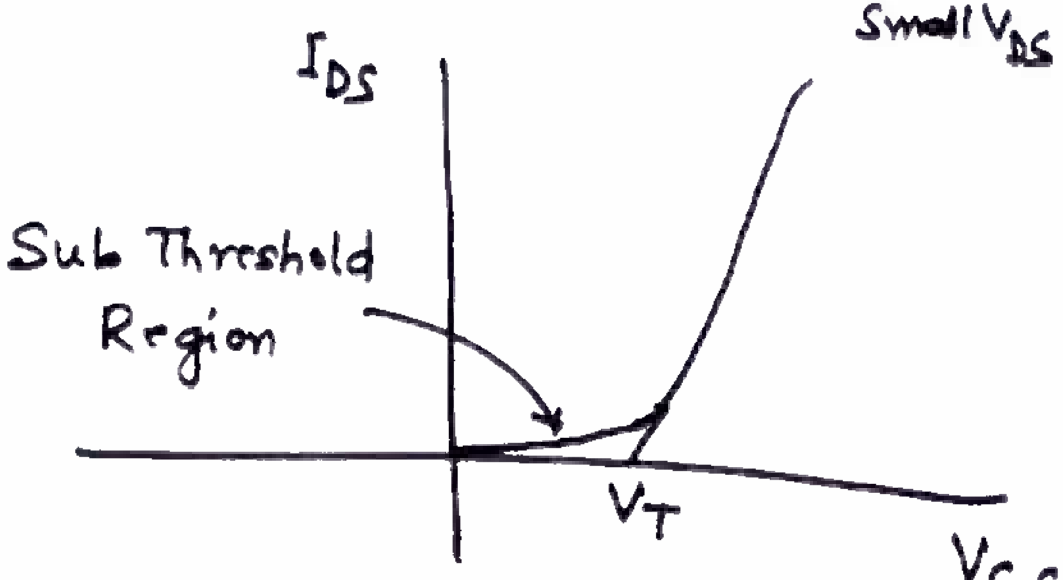


I_{DS} & V_{DS} relation is Parabolic

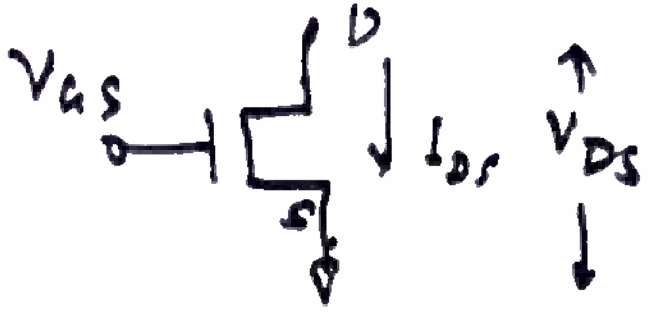
as $$\frac{\partial I_{DS}}{\partial V_{DS}} = \beta'\left(\frac{W}{L}\right)\left[(V_{GS}-V_T) - V_{DS}\right] = 0$$

$\therefore$ Max occures at $\boxed{V_{DS} = V_{GS}-V_T}$

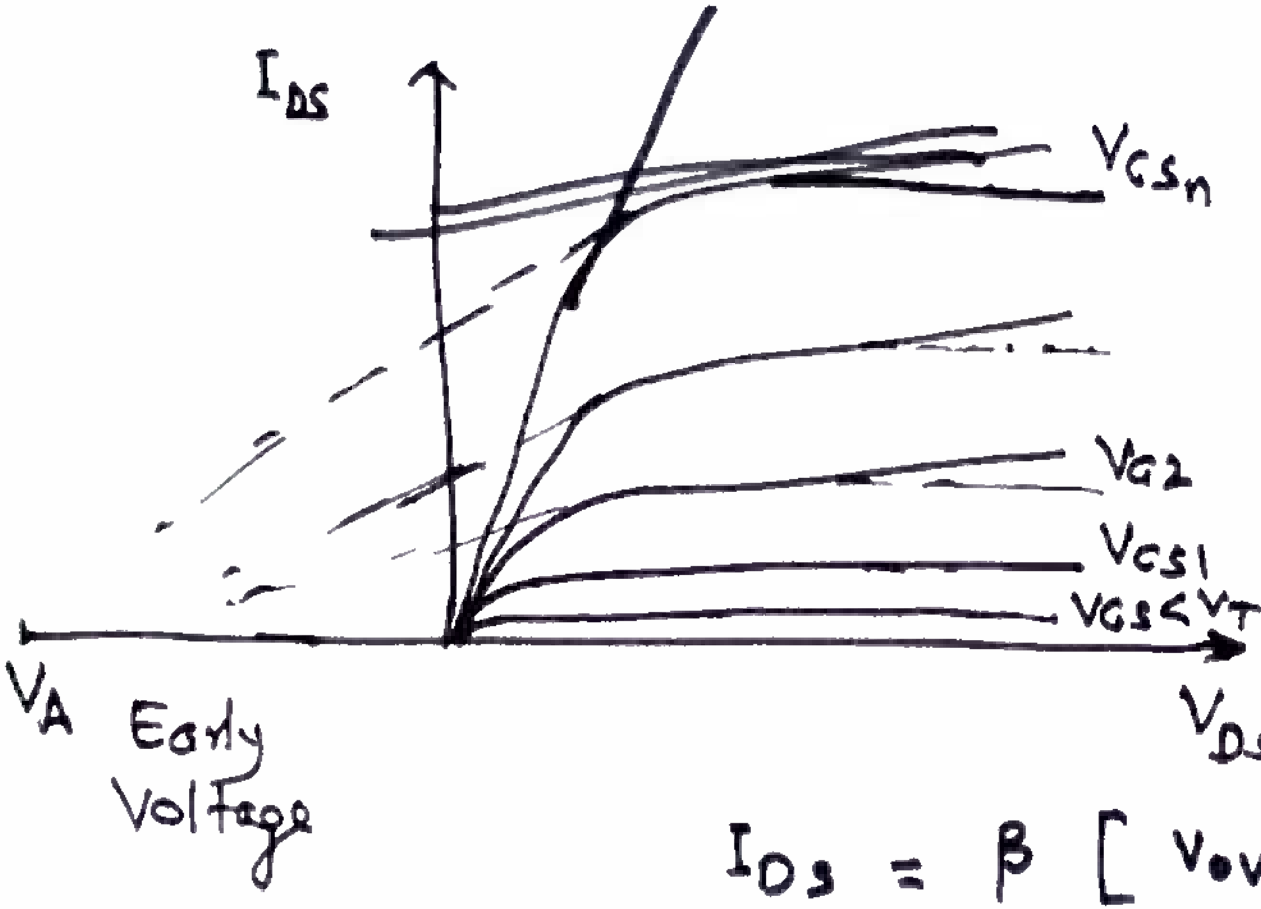
MOSFET I-V characteristics (Input)



NMOS Enhancement



MOS I-V characteristics (output)



$V_{OV} = V_{DS}$

$$I_{DS} = \beta \left[V_{OV} \cdot V_{OV} - \frac{1}{2} V_{OV}^2 \right]$$

$$= \frac{1}{2} \beta V_{OV}^2$$

MOS Transistor Model for Circuits

$$I_{DS} = \mu C_{ox} \left(\frac{W}{L}\right)\left\{\left[V_{GS} - V_T\right] V_{DS} - \frac{1}{2} V_{DS}^2\right\}$$

$$= \beta' \left(\frac{W}{L}\right)\left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

$$= \beta \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

Define $V_{GS} - V_T = V_{GT} = V_{EXC} = V_{OV}$

$V_{OV} > V_{DS}$

Then $I_{DS} = \beta \left[V_{OV} \cdot V_{DS} - \frac{1}{2} V_{DS}^2\right]$

→ Non-saturation Mode

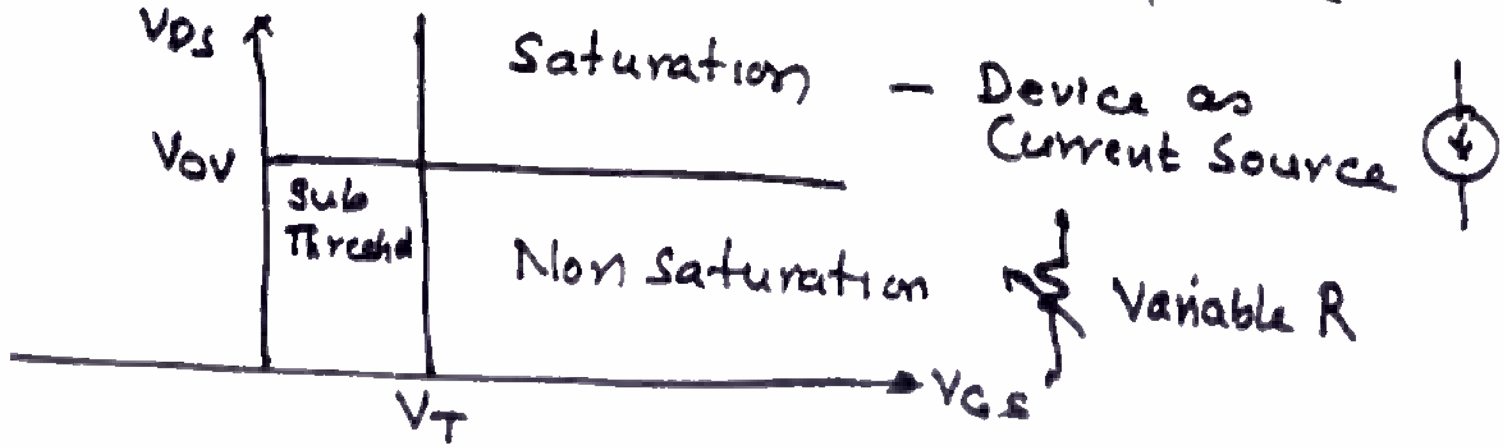
(a) If $V_{ov} > V_{DS}$

Channel exists throughout the Channel Length L. Device is in Linear or Non-Saturation Mode. Device is like

(b) If $V_{ov} \leq V_{DS}$, Channel pinch-off occurs

Then

$$I_{DS} \cong \frac{1}{2}\beta \left[V_{ov}^2 \right]$$ — Saturation Mode



In Saturation:

Slope in $I_{DS}-V_{DS}$ characteristics means

$$I_{DS} \propto V_{DS}$$

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{OV}\right]^2(1+\lambda V_{DS})$$

where λ is saturation parameter and is given by $\lambda = \frac{\lambda'}{L}$

where $\lambda' \cong \sqrt{\frac{2}{q N_{substrate}}}$

$\therefore \lambda \propto \frac{1}{L}$

shorter channel length devices have larger λ

Hence Transistor is Modeled by Two Equations

$$I_{DS} = \mu_n C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$= \beta\left[V_{ov}\cdot V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad -[A]$$

when $V_{GS}-V_T > V_{DS}$

i.e. Device is in Non Saturation Mode

Clearly if V_{DS} is small $I_{DS} \propto V_{DS}$ i.e. Linear Mode

or $\frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{\beta(V_{GS}-V_T)}$ => Resistive Behaviour

which mean for different values of V_{GS}

$R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}}$ varies inversely as V_{GS} increases.

Equivalent Circuit  Non linear Resistor

In Saturation, with λ smaller

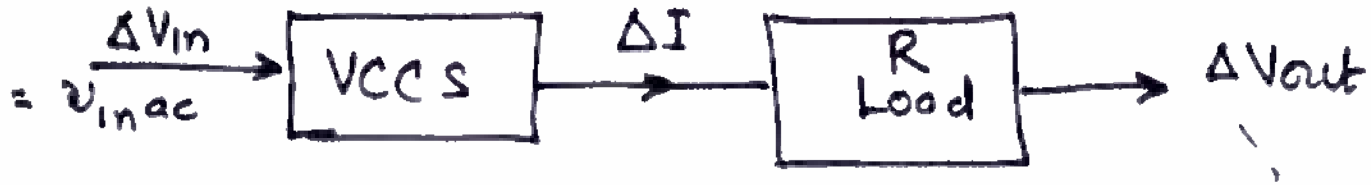
$$I_{DS} = \frac{1}{2} \beta V_{OV}^2$$

$\neq f(V_{DS})$ $\therefore$ Device acts as

Constant current source which Voltage Controlled Source.

called VCCS $\Rightarrow$

An Amplifier (Voltage Amplifier here) can be represented as



$$\text{Gain} = \frac{\Delta V_{out}}{\Delta V_{in}}$$