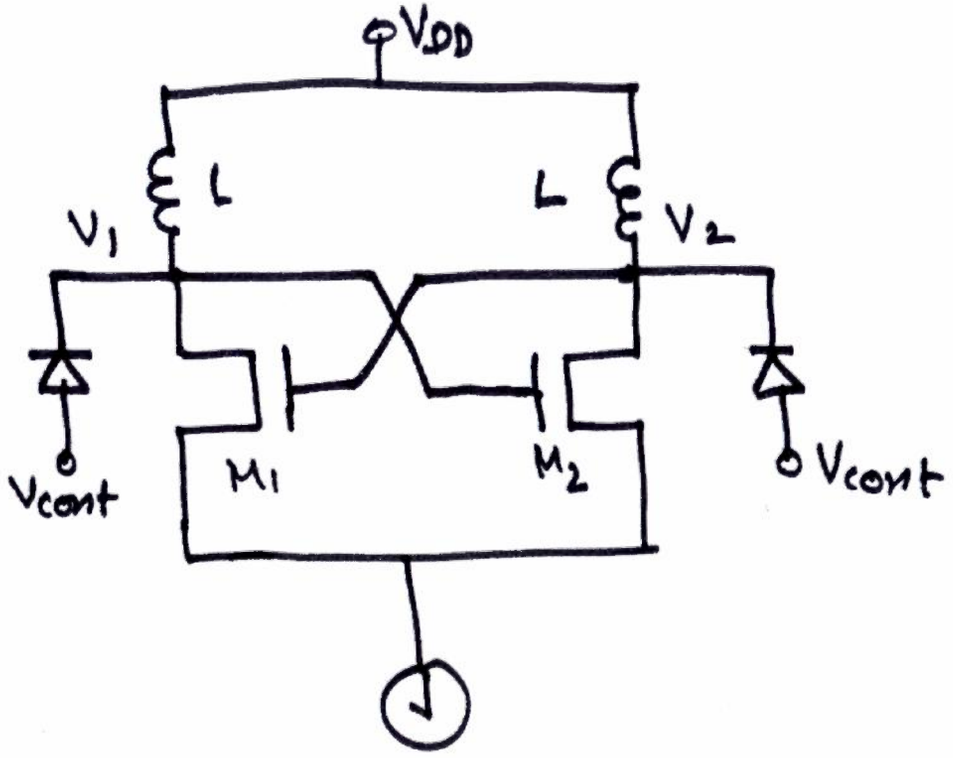
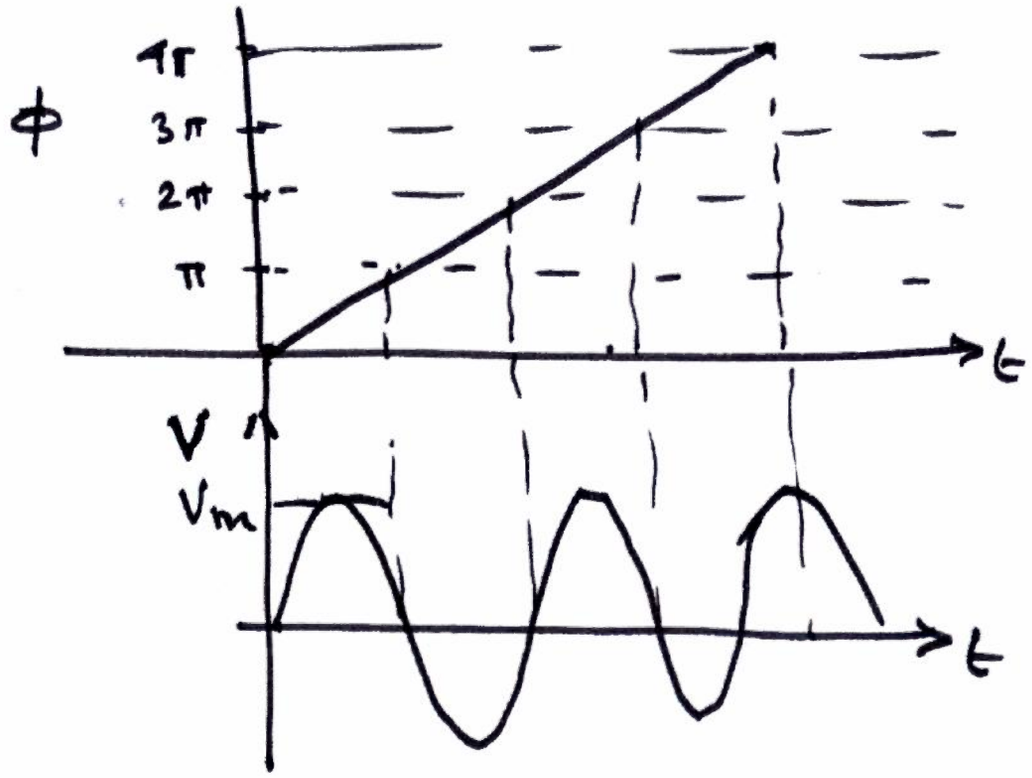
Tuning LC Oscillator



$$C_{Varactor} = \frac{C_0}{\left(1 + \frac{V_R}{\phi_B}\right)^m}$$

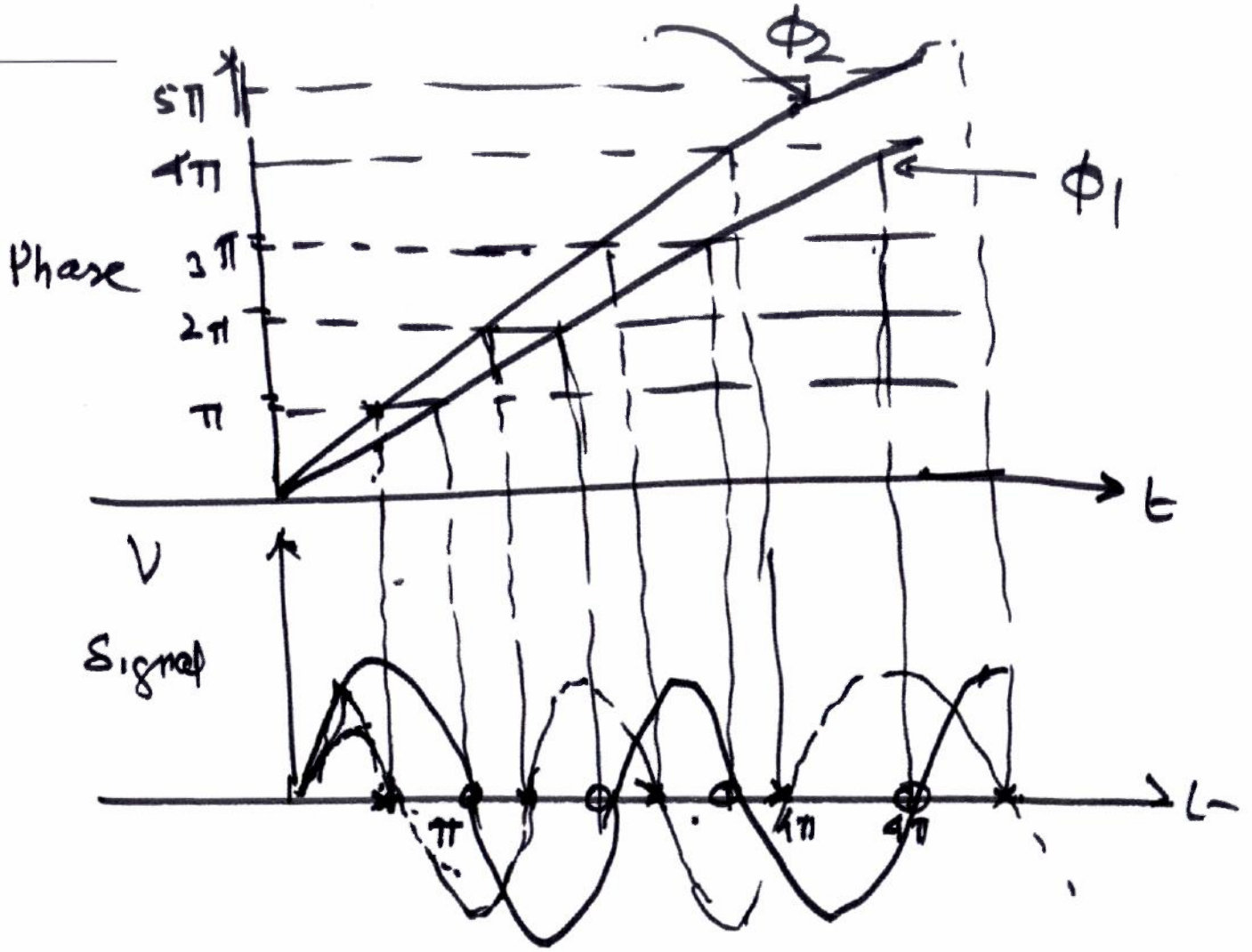
$m = 0.4$ to 0.5

Mathematical Model of VCO



$$\omega = \frac{d\phi}{dt}$$

$$\omega t = \phi$$



$$\therefore \boxed{\frac{d\phi}{dt} = \omega}$$

$$\phi = \int \omega dt + \phi_0$$

In a VCO

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$$

We have oscillator output—

$$V_0(t) = V_M \cos \phi t = V_M \cos \int \omega_{out} dt + \phi_0$$

$$\text{or } V_{out}(t) = V_M \cos\left\{\omega_0 t + K V_{co} \int V_{cont}\, dt + \phi_0\right\}$$

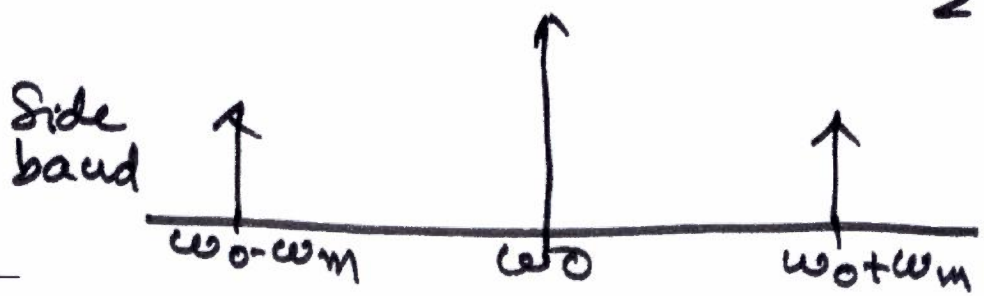
Assume $\phi_0 = 0$

& $V_{cont} = V_m \cos\omega_m t$ (If V_{cont} Varies)

$$\text{Then } V_{out}(t) = V_M \cos\left\{\omega_0 t + K_{VCO} \int V_M \cos\omega_m t\, dt\right\}$$

$$\cong V_M \cdot \cos\omega_0 t - V_0 (\sin\omega_0 t)\left(K_{VCO} \frac{V_m}{\omega_m} \sin\omega_m t\right)$$

$$= V_M \cos\omega_0 t - \frac{K V_{co} V_M V_m}{2\omega_m}\left[\cos(\omega_0 - \omega_m)t - \cos(\omega_0 + \omega_m)t\right]$$



Phase Lock Loop

PLL was invented in 1930

1. Locking VCO to a Frequency

2. Frequency Synthesizers

3. Used in Mobile phones, TV, Receivers, Pager, Telephony

(a) Digital PLL — 1965 - 1970 (b) Sinusoidal PLL

(c) Optical PLL 1965

Definition:A PLL is a Feedback system
That
Compares the Output Phase
With
The Input Phase.
Comparison is performed
By
PHASE COMPARATOR

Analog Designers find issues related to

(a) Jitter

(b) Phase Noise

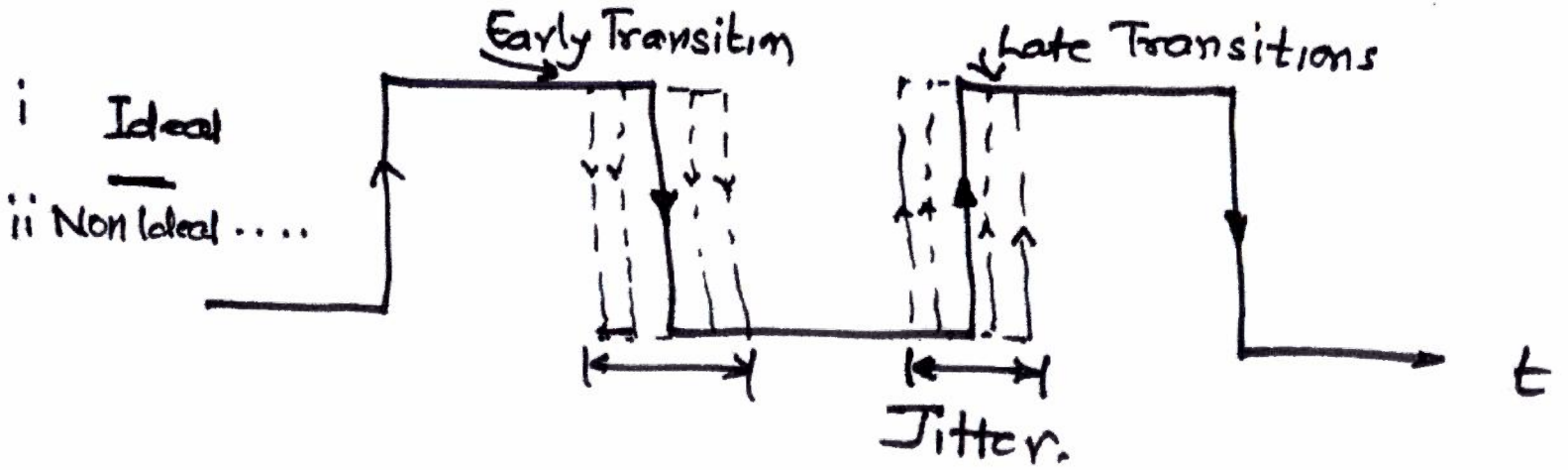
CDEEP
IIT Bombay

very difficult to handle at high frequencies, which are now used in most Electronic & Communication Systems. Even Digital Systems on Board (PCB) also get critically affected due to two parameters or characteristics as above.

Example : 100 MHz Pulse waveform (50% Duty cycle), show period of 10 psec and alternating at 5 psec at every edge.

But this is only an Ideal Case

Transitions normally do not occure at 5 psec edge and that creates, what we term as Jitter



Jitter :— i Deterministic
ii Random

i. Deterministic :— Cross talk

EMI radiation on Signal Path

Noise from surroundings

Switching — Power supply Droop
Ground Bounce

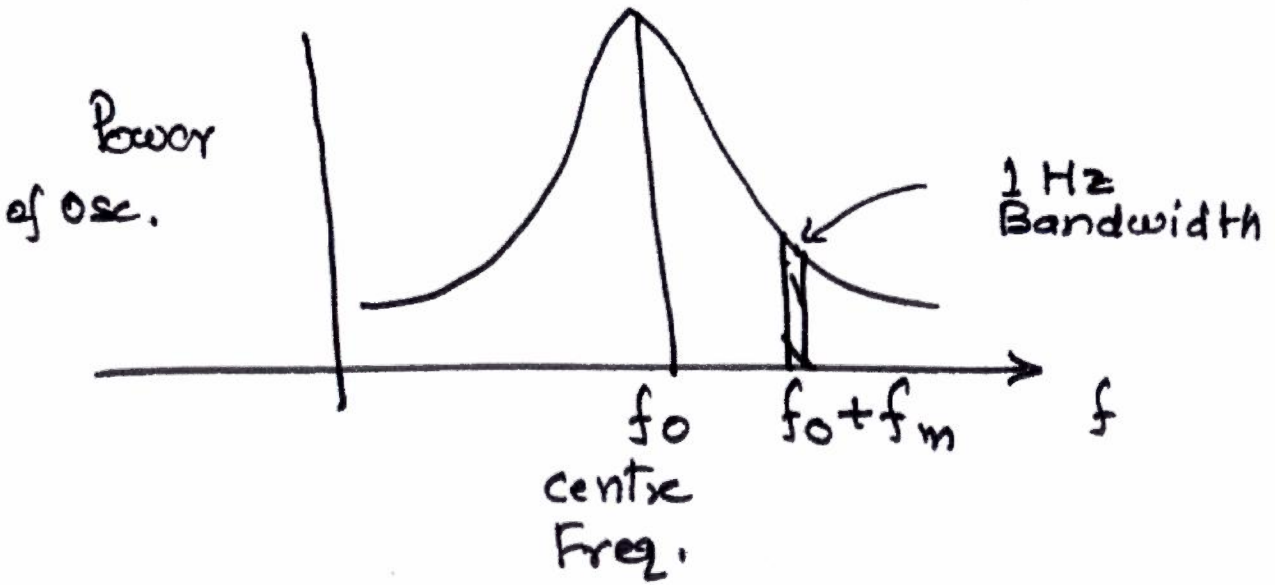
ii Random :— Temperature, Process Variations,
Interface states

Random Jitter is Gaussian in nature

Multiple random jitter sources add to RMS Jitter.

Phase Noise :

Variation in Signal timings can also be represented in Frequency Domain and resultant Noise distribution is measured as Phase - Noise (PN)

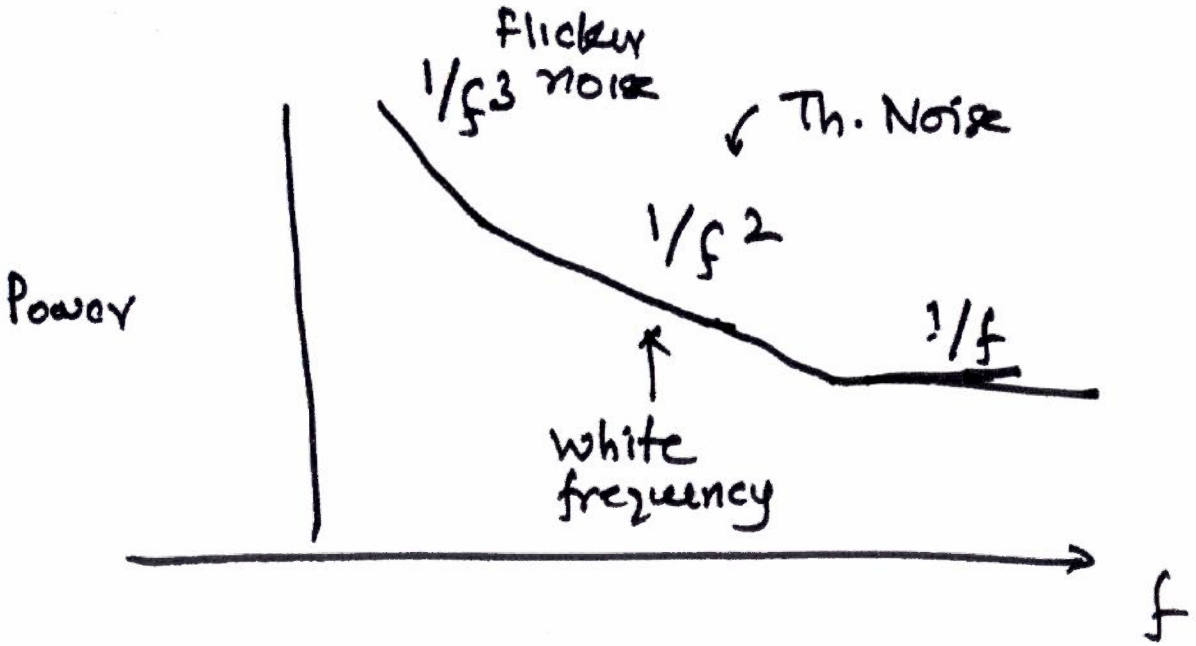


If PN is = 0
Then all Oscillator Power goes to 'fo'

But PN spread some power to adjoscent frequencies, which results in Sidebands.

$$\text{Phase Noise} = \frac{\text{Power in 1 Hz Bandwidth at Offset freq}}{\text{Total Power of the Carrier}}$$

$$= \text{dBc/Hz}$$



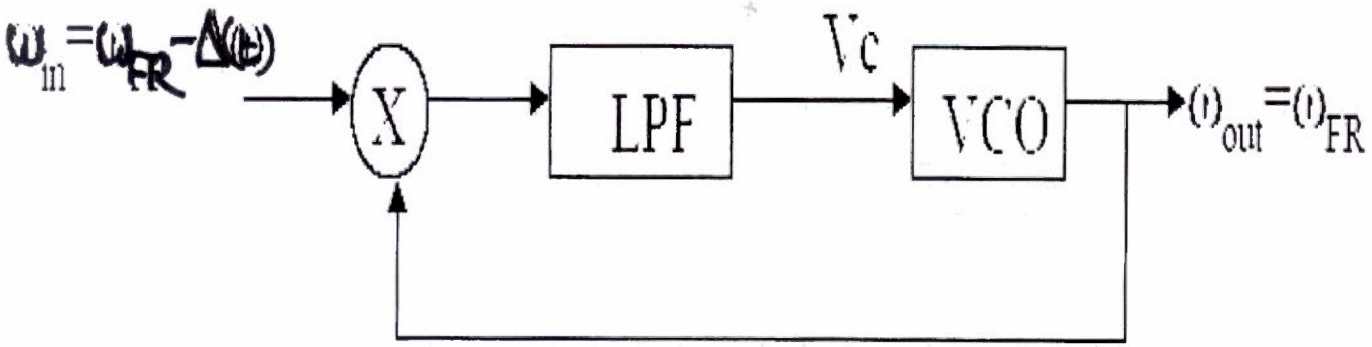
17 Terminology

Frequency Locked

Phase error < permissible phase error (e.g. 1.5% of the output freq.)

Pull-in range (Capture Range)

The frequency range over which a loop can acquire lock.



15

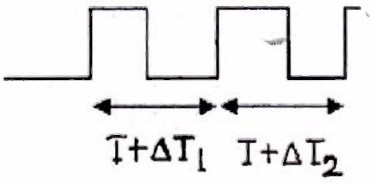
Terminology

Jitter :

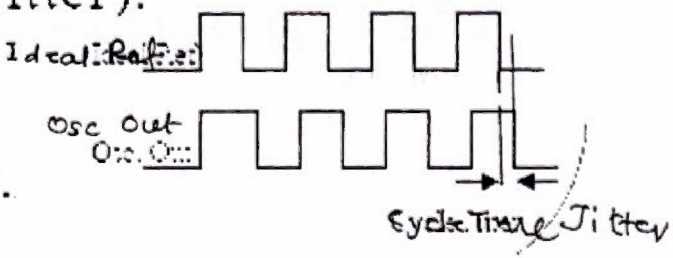
① Deterministic.

Random - specified in rms value or peak to peak

Cycle to cycle jitter.



Accumulated jitter (cycle jitter).



③

Duty cycle distortion jitter.

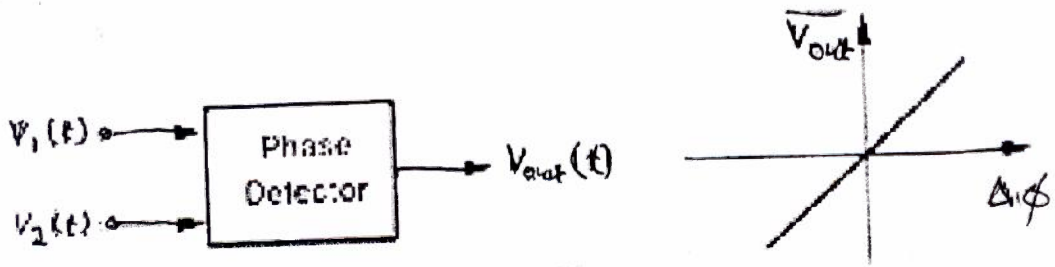
Basic

ic PLL

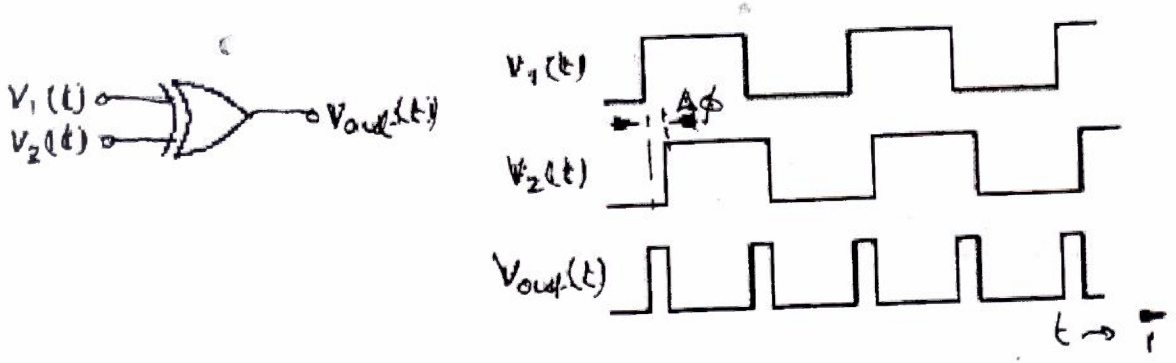
Phase —

ise Detector

Phase Detector



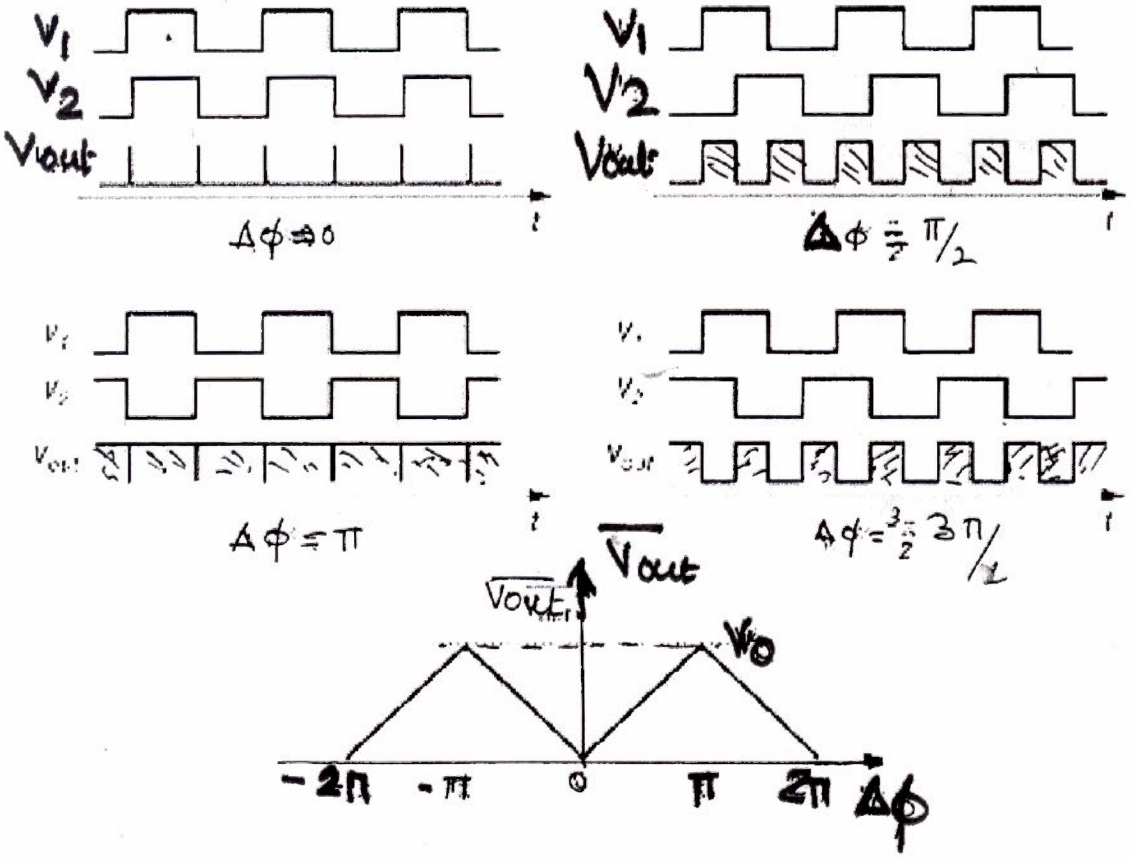
Definition of Phase detector



XOR gate as phase detector

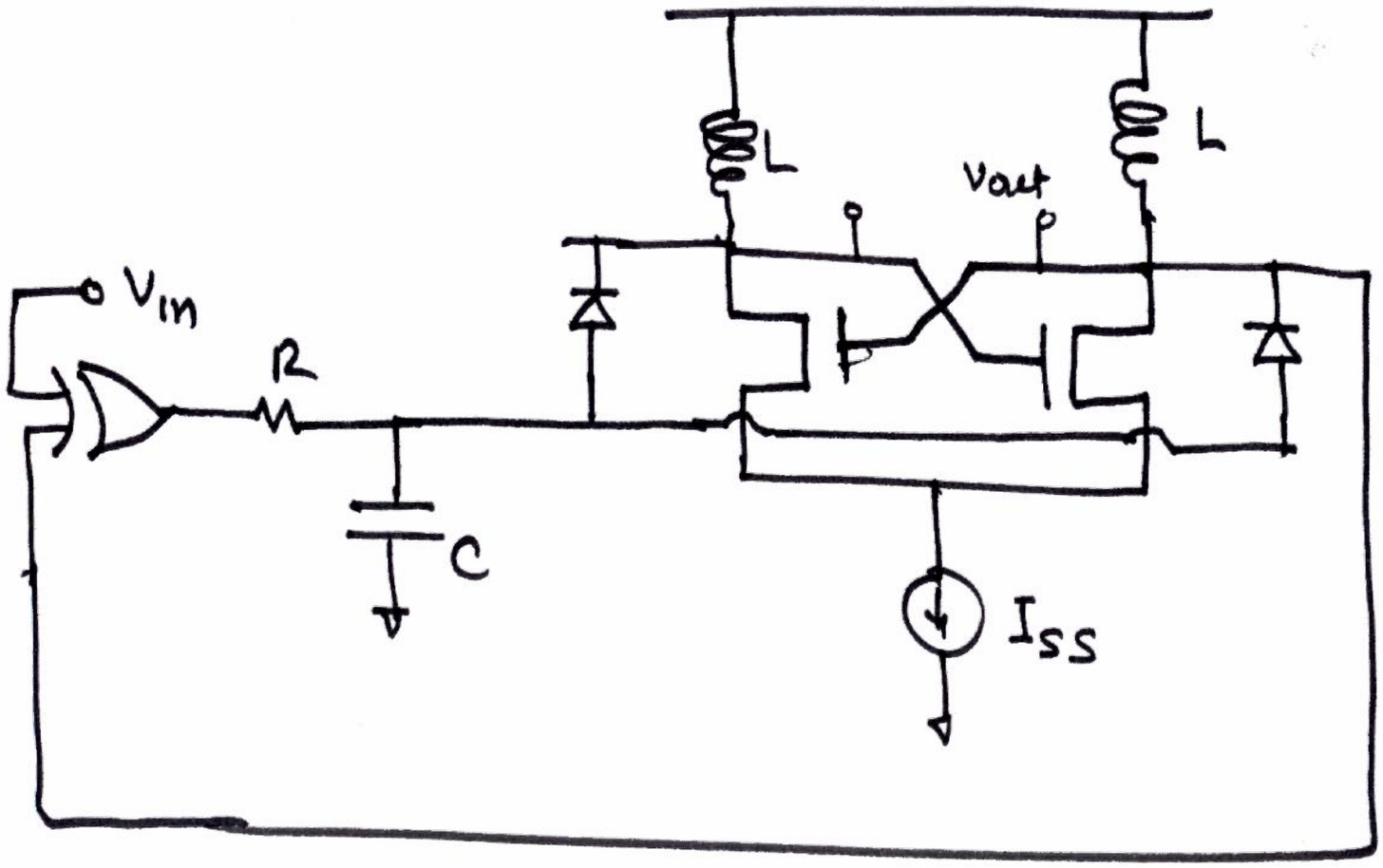
Ref. (Razavi)

Simple PLL



Phase detector output for different input skews

A Typical PLL in CMOS



-gm (LC) oscillator