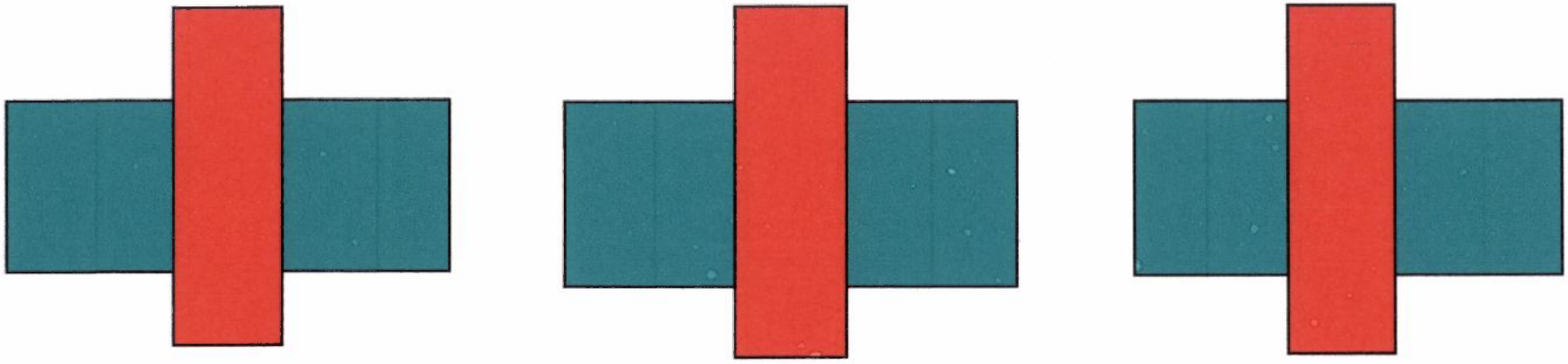
Transistor mismatch in deep sub-micron technology

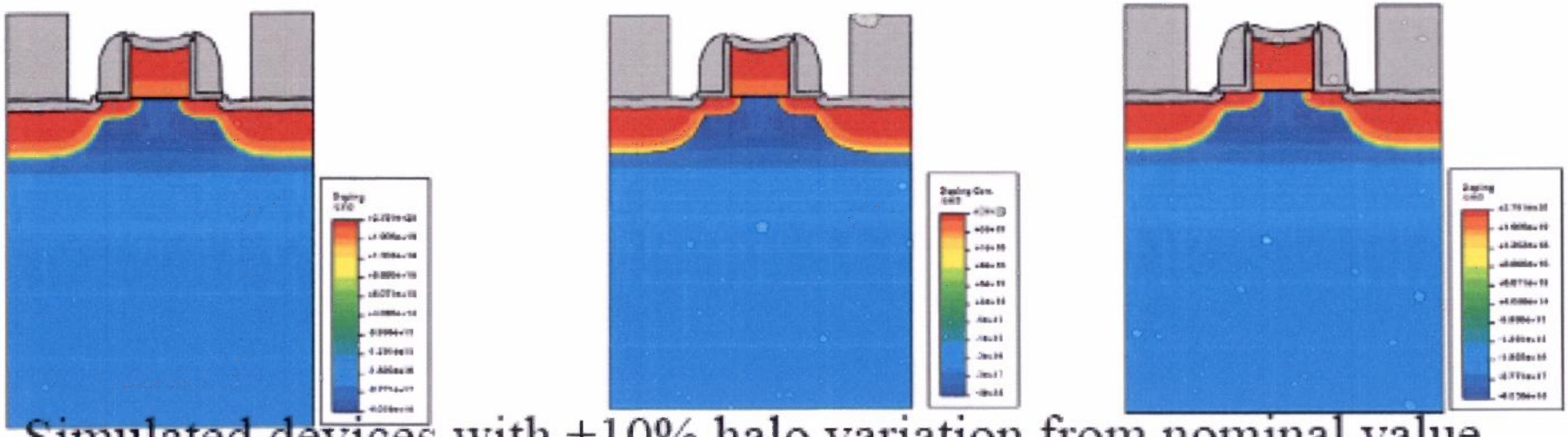
- Factors causing transistor mismatch
- Modeling the transistor mismatch
- Controlling mismatch effect at process/device level
- Impact of transistor mismatch in sense-amplifier design
- Controlling mismatch effect at circuit level

Transistor Mismatch Effects

3 identical transistors in a chip at the circuit design phase



The structure of 3 transistors after the completion of IC processing



Simulated devices with ±10% halo variation from nominal value

Factors Causing Mismatch

1.*Intrinsic type*

- Discrete dopant effect
- Interface state density fluctuations

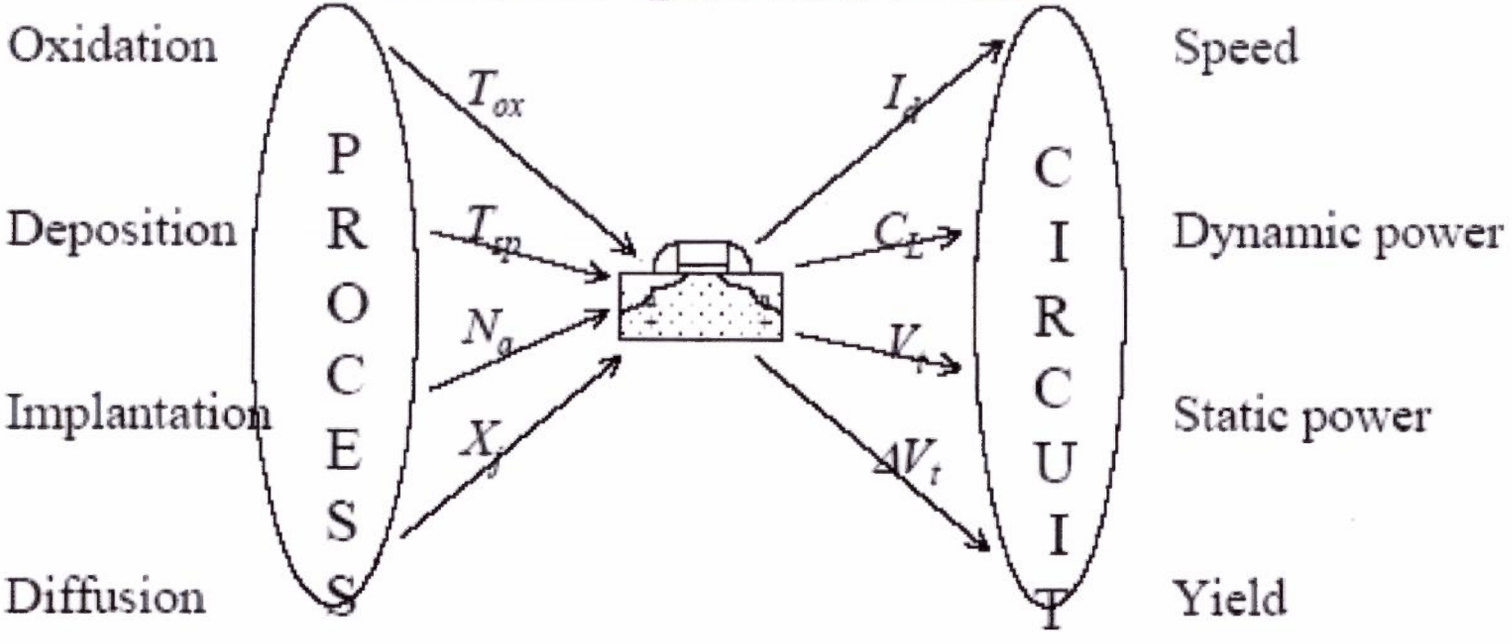
2.*Extrinsic type due to random variation in:*

- Gate length and width
- Oxide thickness
- Implant dose
- Implant energy
- Anneal temperature
- Gate & S/D overlap
- Spacer thickness

Device parameters affected by process parameters

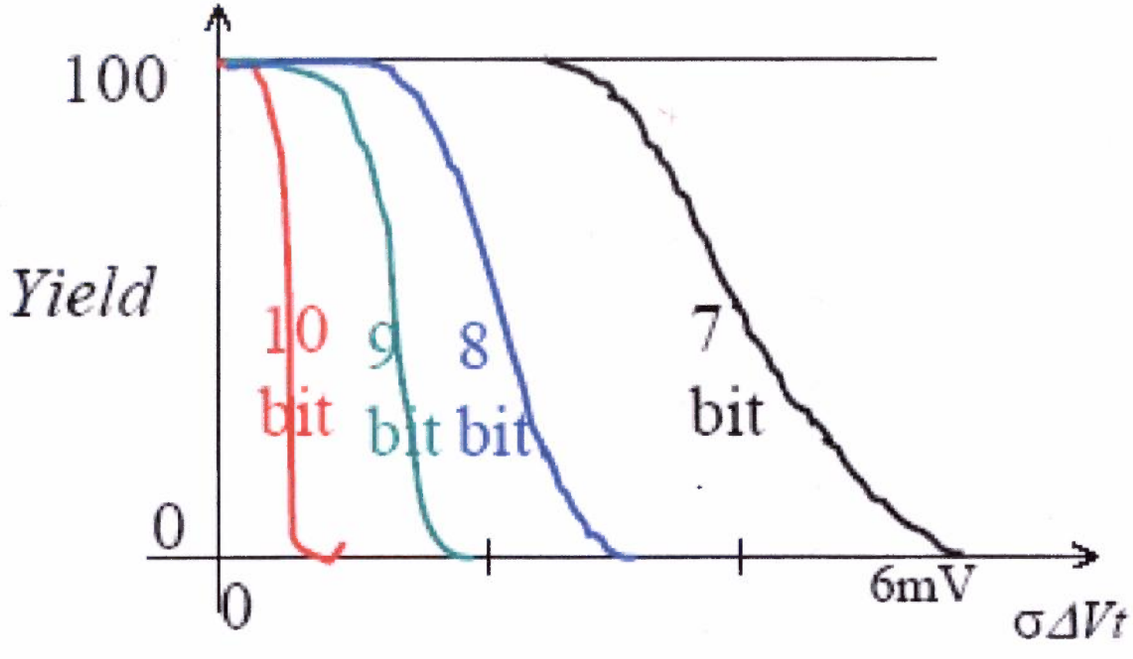
- I_{off}, the leakage current
- I_{on}, the saturation current
- V_t, the threshold voltage
- S, the Sub threshold slope
- g_m, the Tranconductance.
- Various R s, C s and parasitics

Impact of process parameters on circuit parameters



- Circuit performance has a direct relation on process in a complex way.
- The relation between circuit parameter to process parameter is highly nonlinear.
- Some of the Process level parameters are statistically correlated. Faiz et al

ADC Yield



The higher precision requires very low mismatch

The yield for high precision drops off very fast

Layout Issues

Orientation

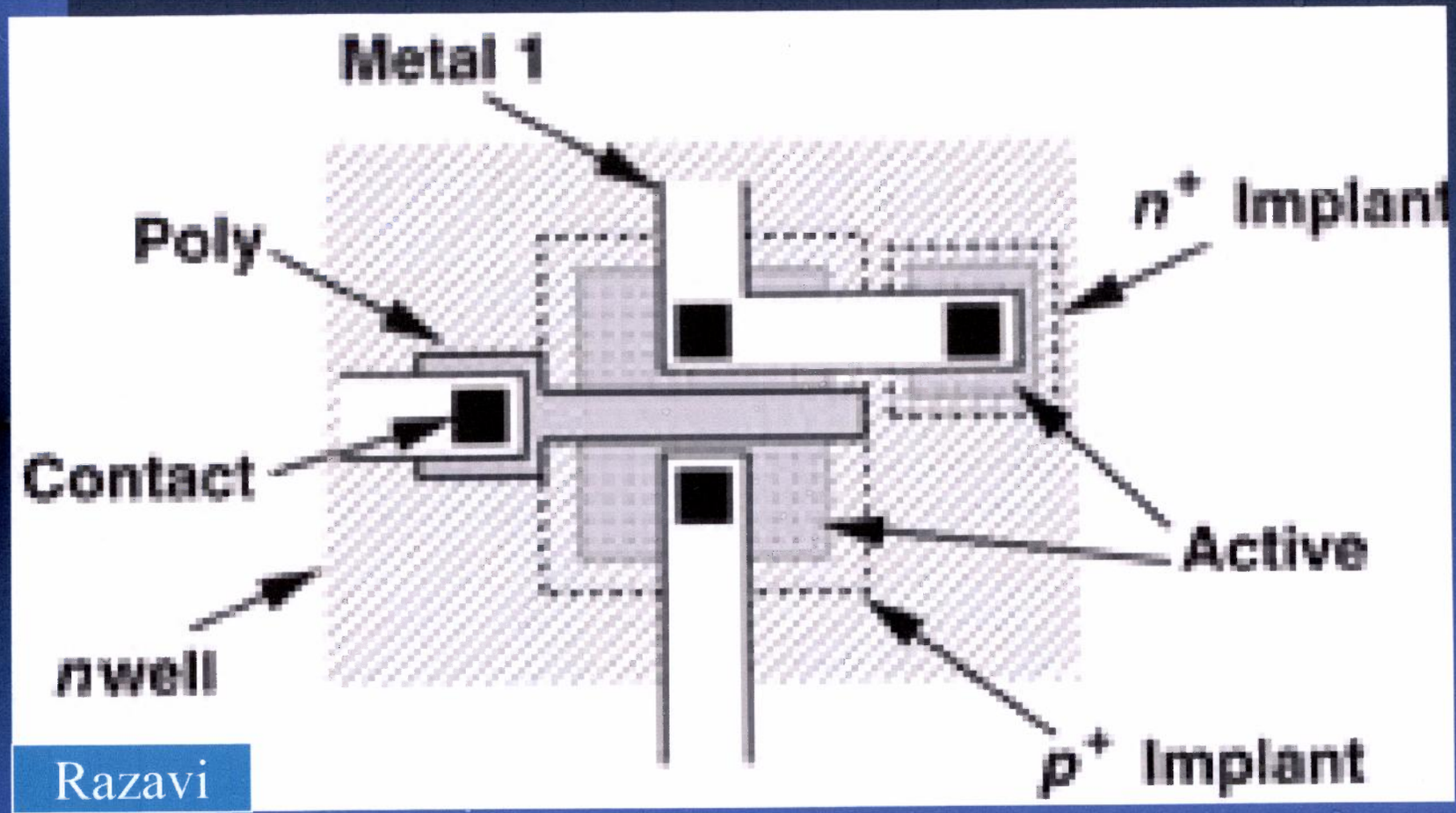
Symmetry

Adding dummy layers

Unit cell repetition

Common centroid

Avoiding interconnect resistance


Metal 1
Poly
Contact
nwell
n+ Implant
Active
p+ Implant
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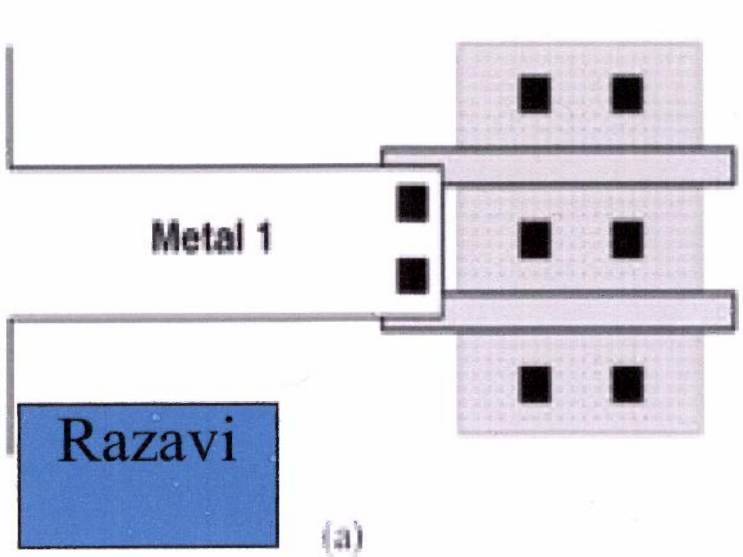
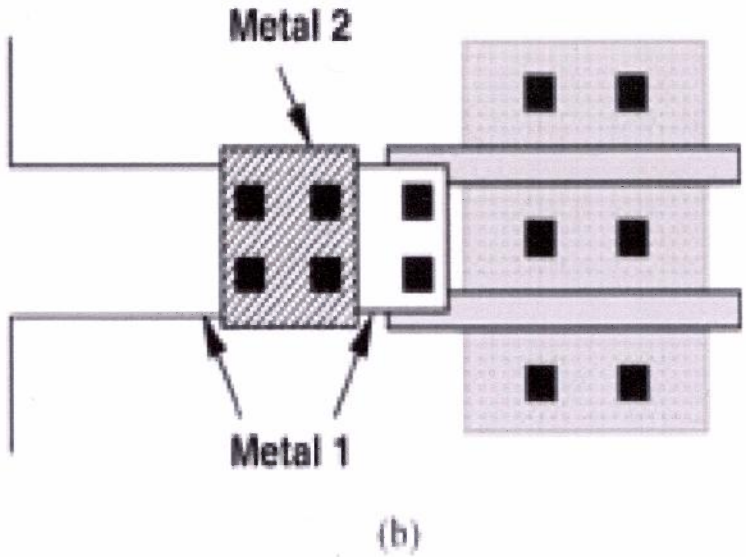
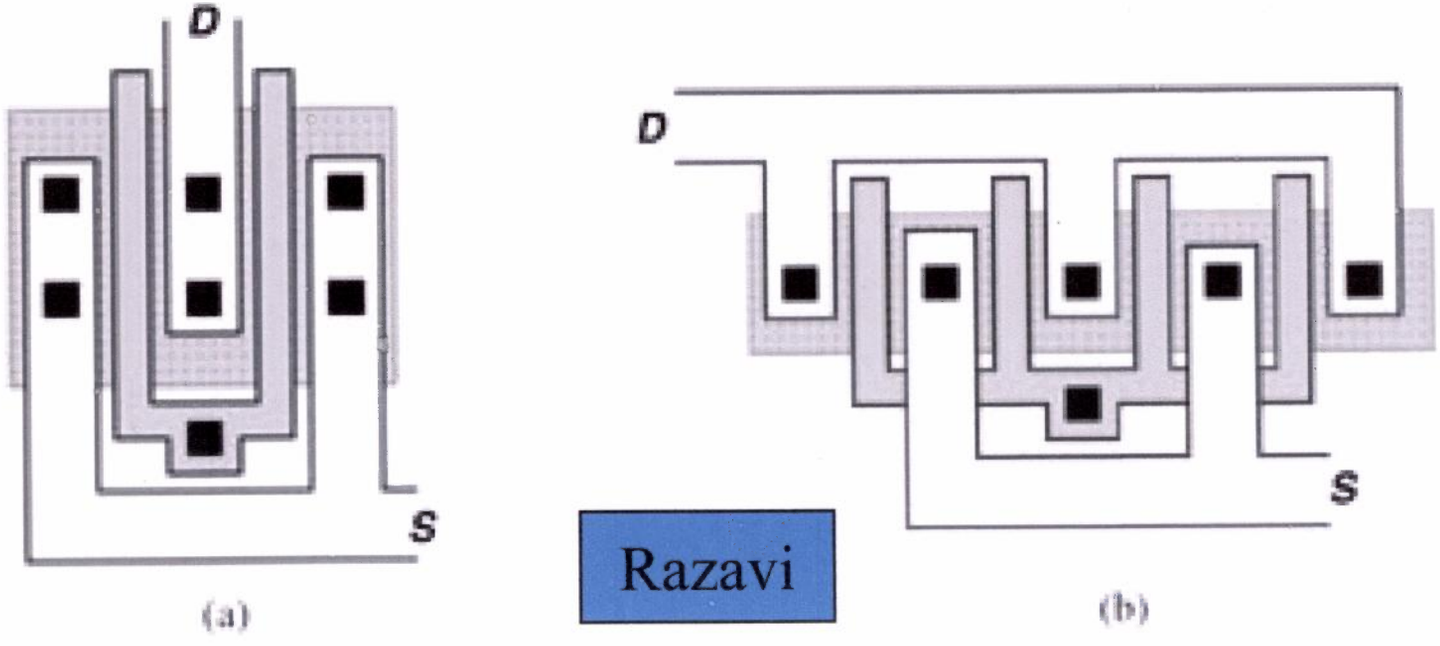
Antenna Effect





Folding of MOSFET

Multi-Finger Transistors



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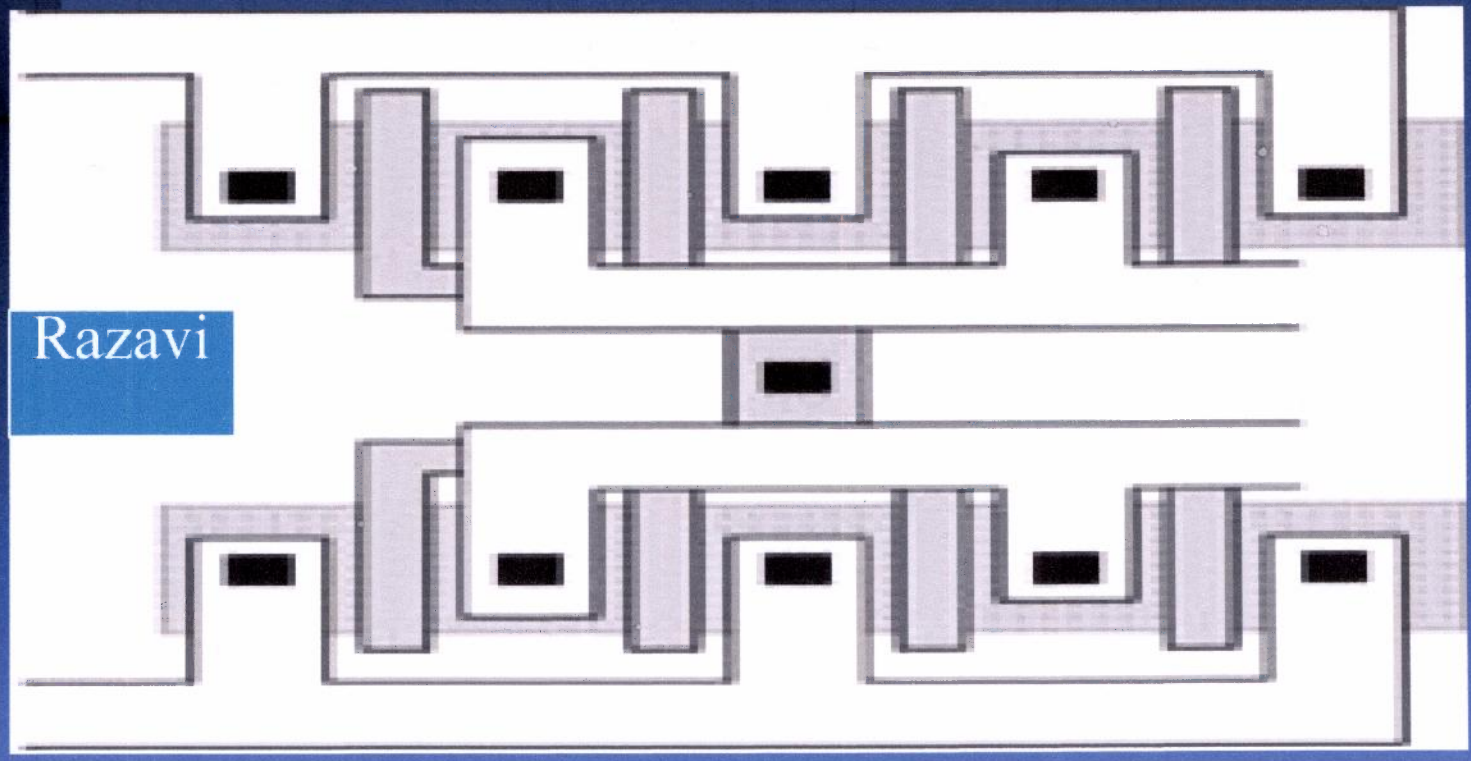
WIDE Transistor

Many finger

Layout



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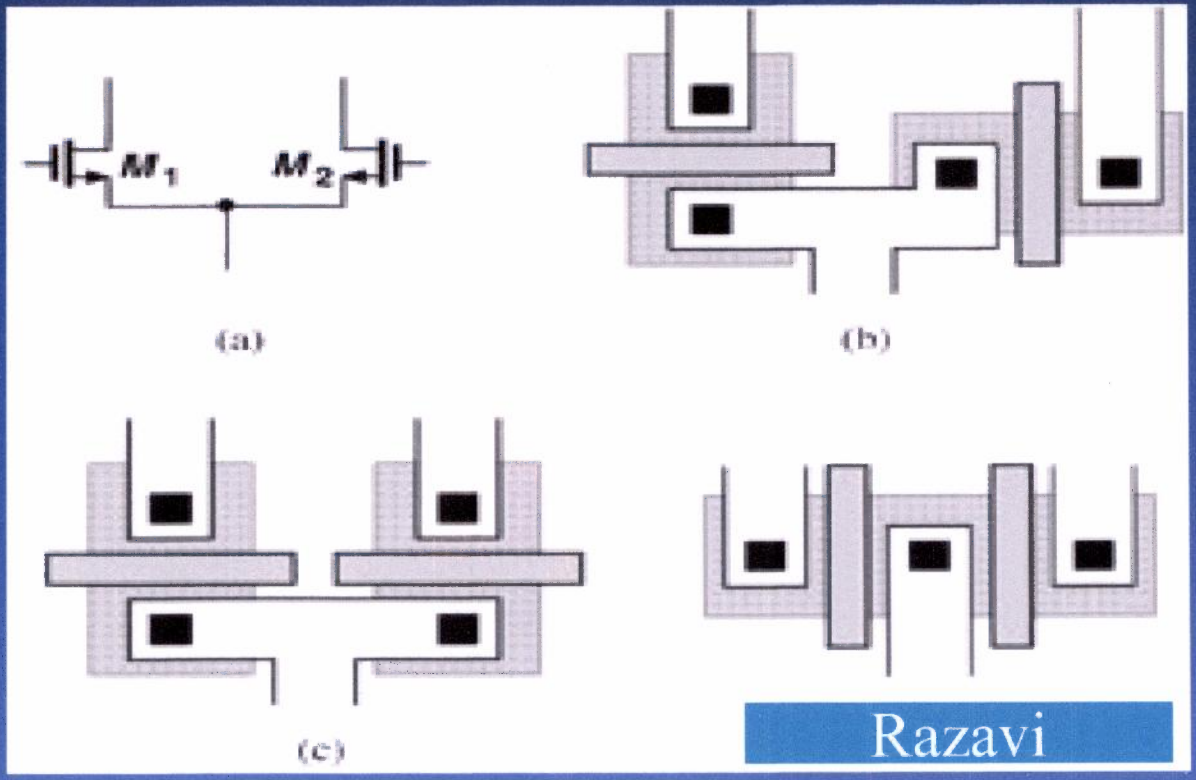
DIFFERENTIAL PAIR

(b)Different orientations

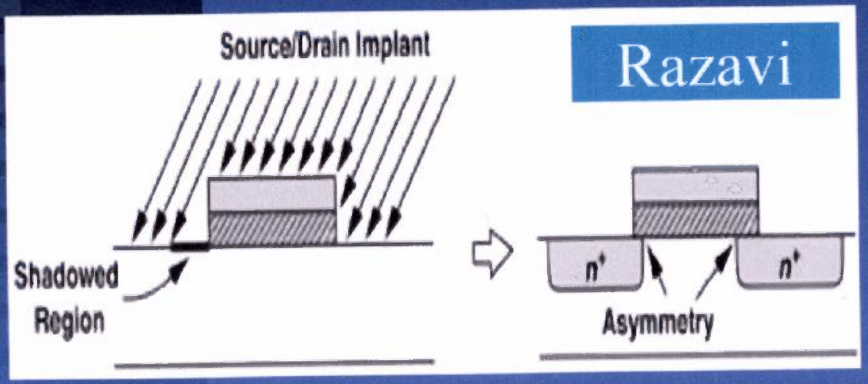
(c) Gate Aligned

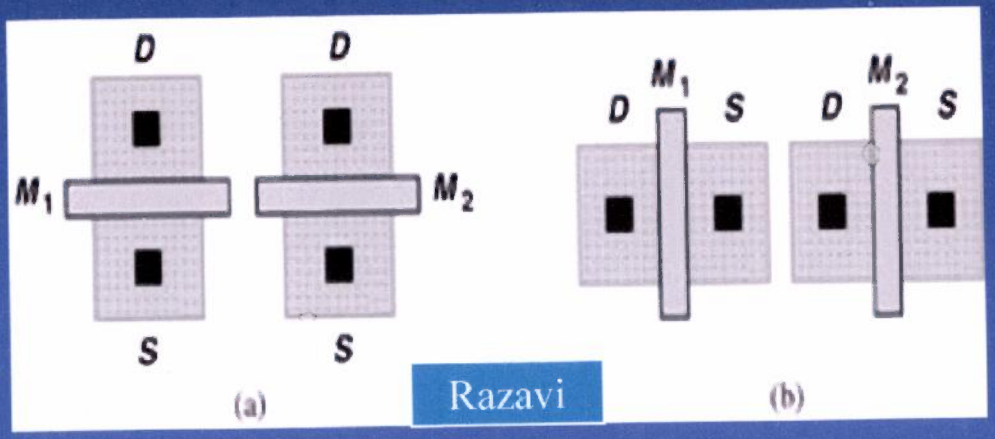
(d)Parallel Gates



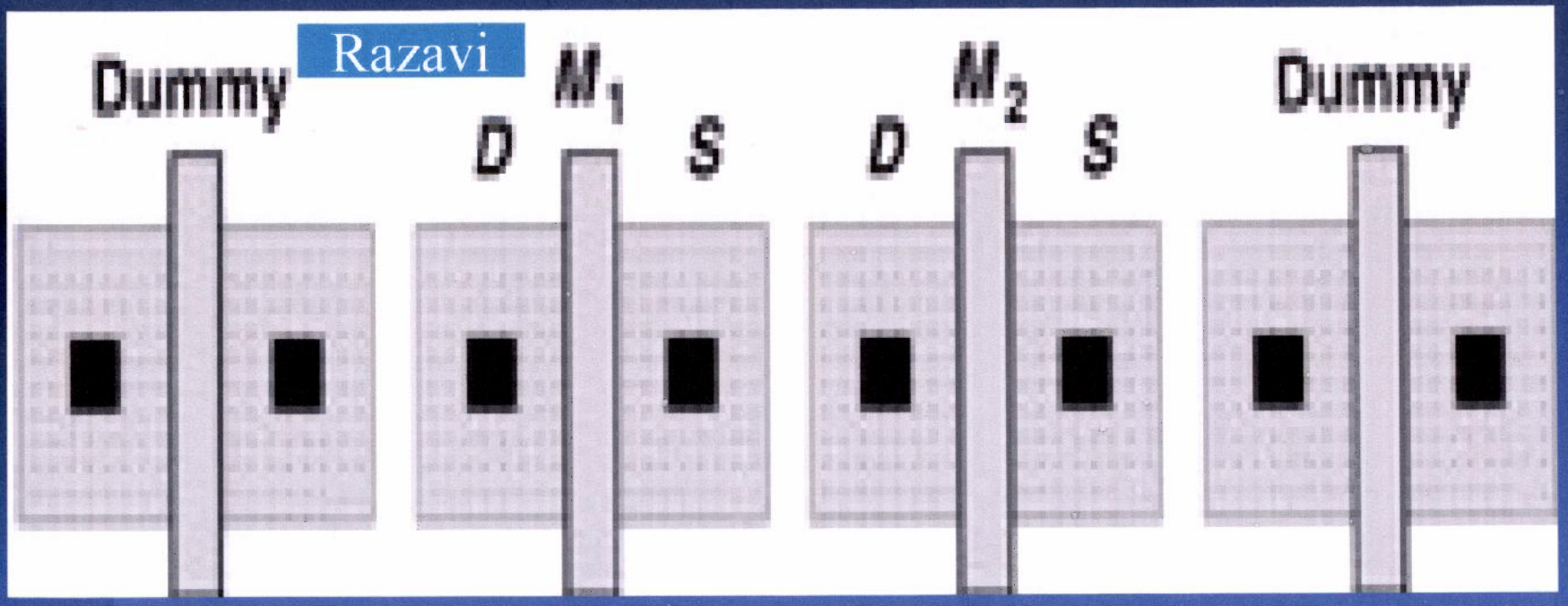
Effect of Gate shadowing

Gate Aligned Vs. Parallel Gates



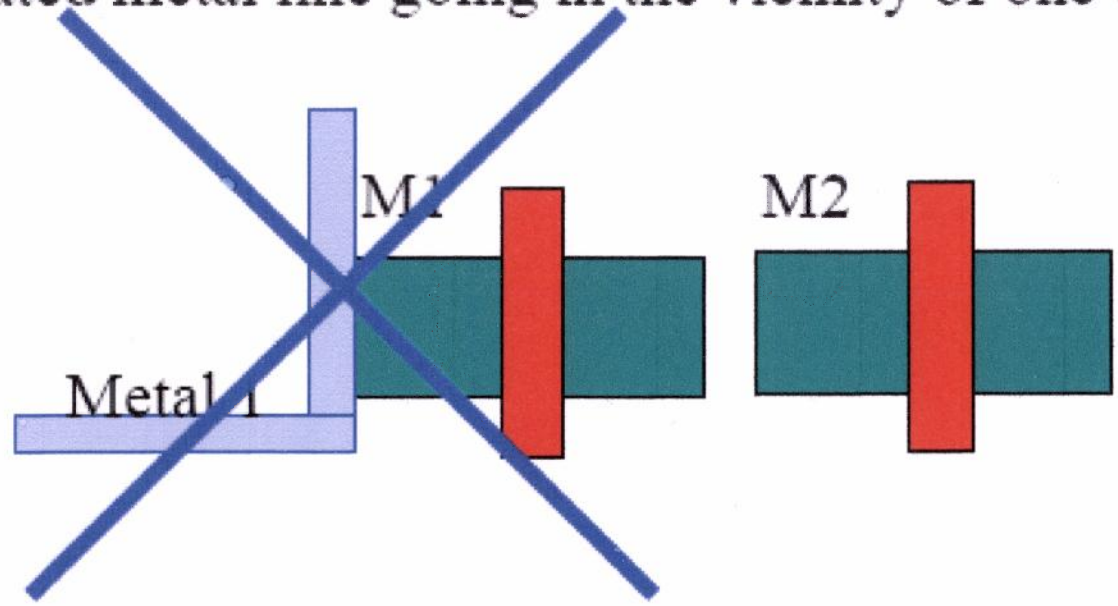


Dummy Devices Added

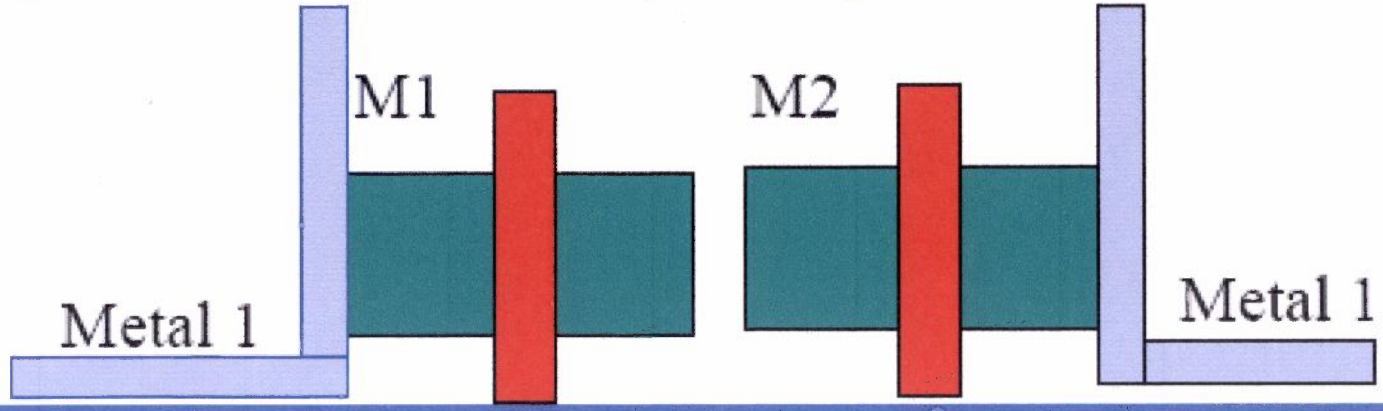


Symmetry

An unrelated metal line going in the vicinity of one of the transistor

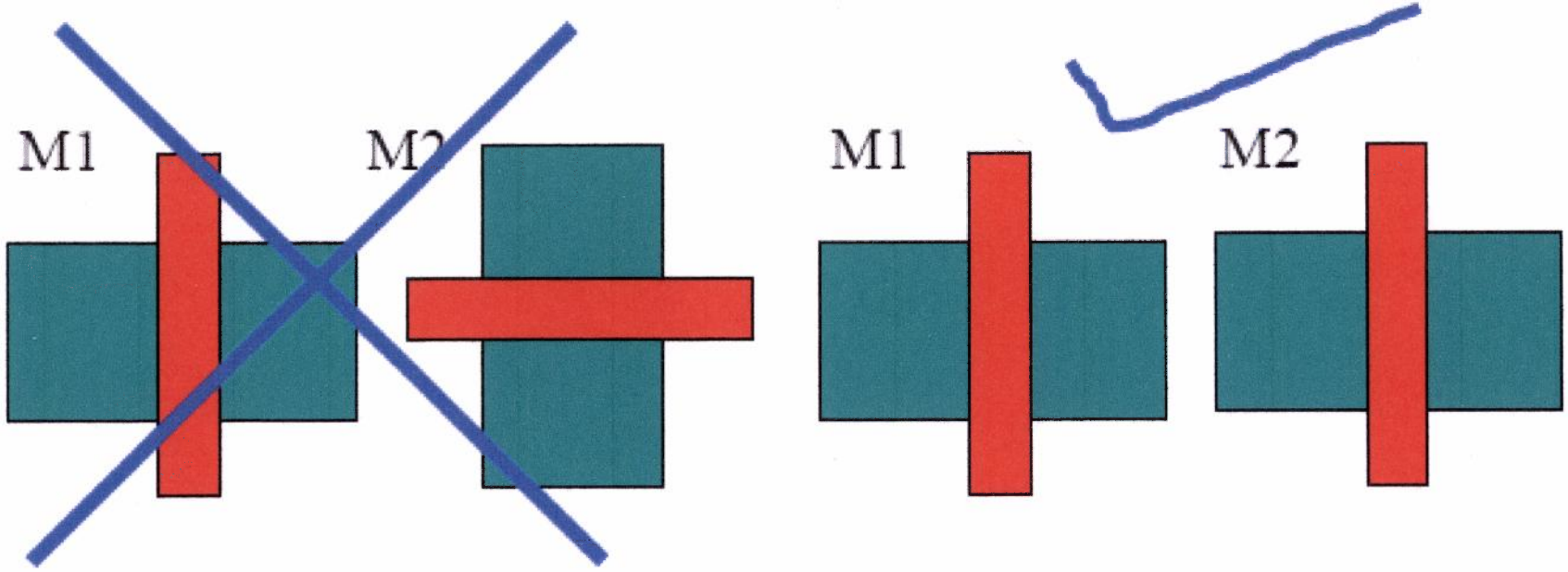


Symmetry should be preserved by adding another similar line



Orientation

Matched transistors should be oriented in same direction



Photolythography process has different biases in different axes, hence the requirement

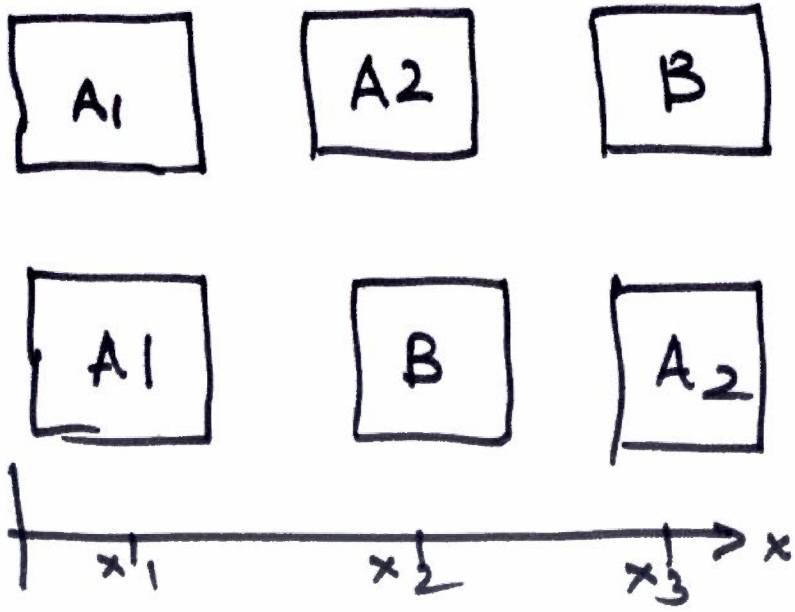
Linear Gradient Problem

Size of A = 2 · Size of B.

Gradient →

Assuming Gradient is Linear

$y = mx + c$



$A1 = mx_1 + b$

$A2 = mx_2 + b$

$B = mx_3 + b$

$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_2) + 2b}{mx_3 + b}$$

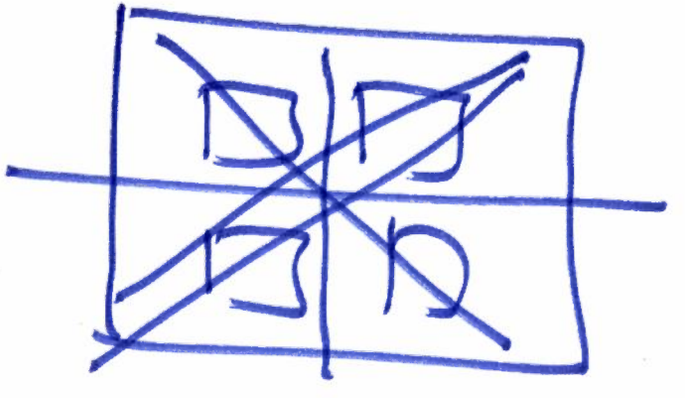
If $x_3 \neq \frac{x_1+x_2}{2}$

Then $\frac{A_1+A_2}{B} \neq 2$

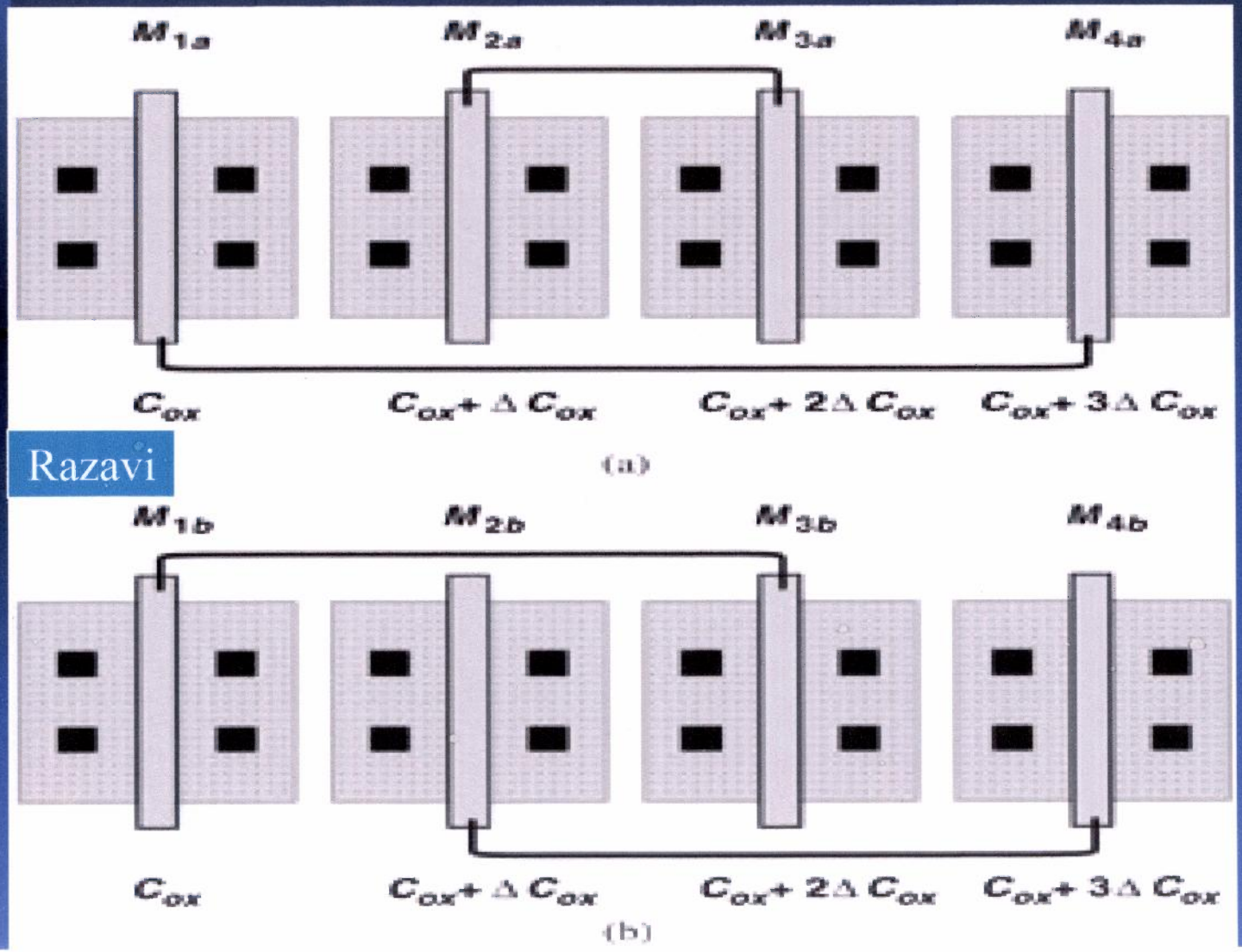
However if $x_1 - x_2 = x_2 - x_3$

or $x_2 = \frac{x_1+x_3}{2}$

Then Matching is Possible.



One Dimensional Cross-coupling



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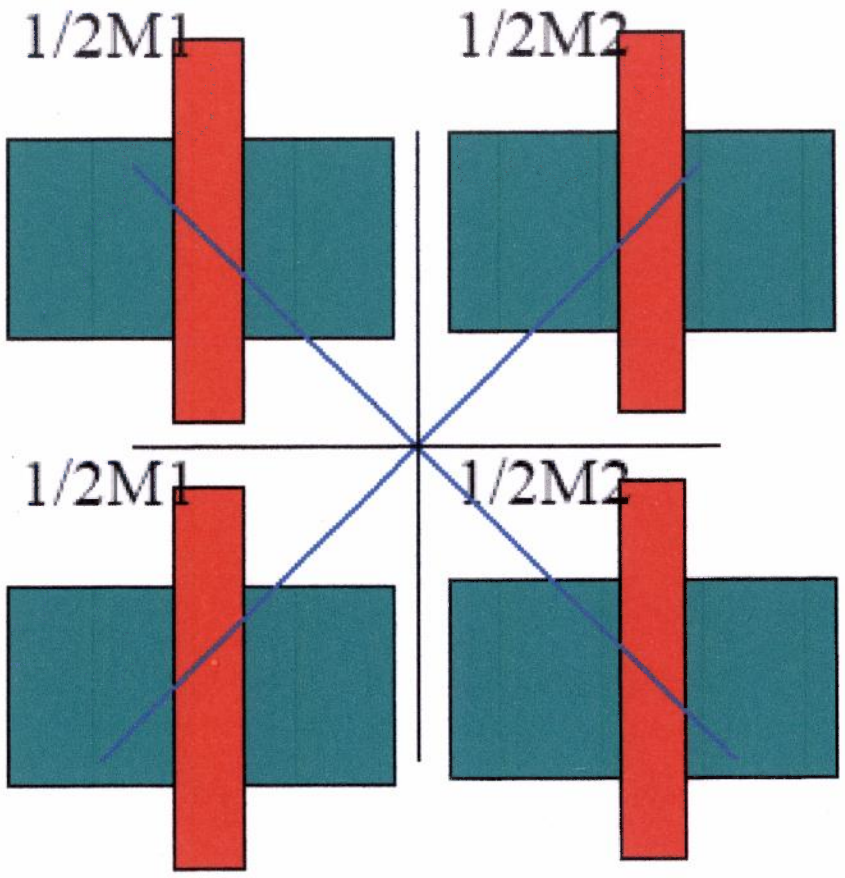
Common centroid



Common centroid configuration eliminates the first order gradient effects of parameters along both the axes

Use of n-Well Resistors

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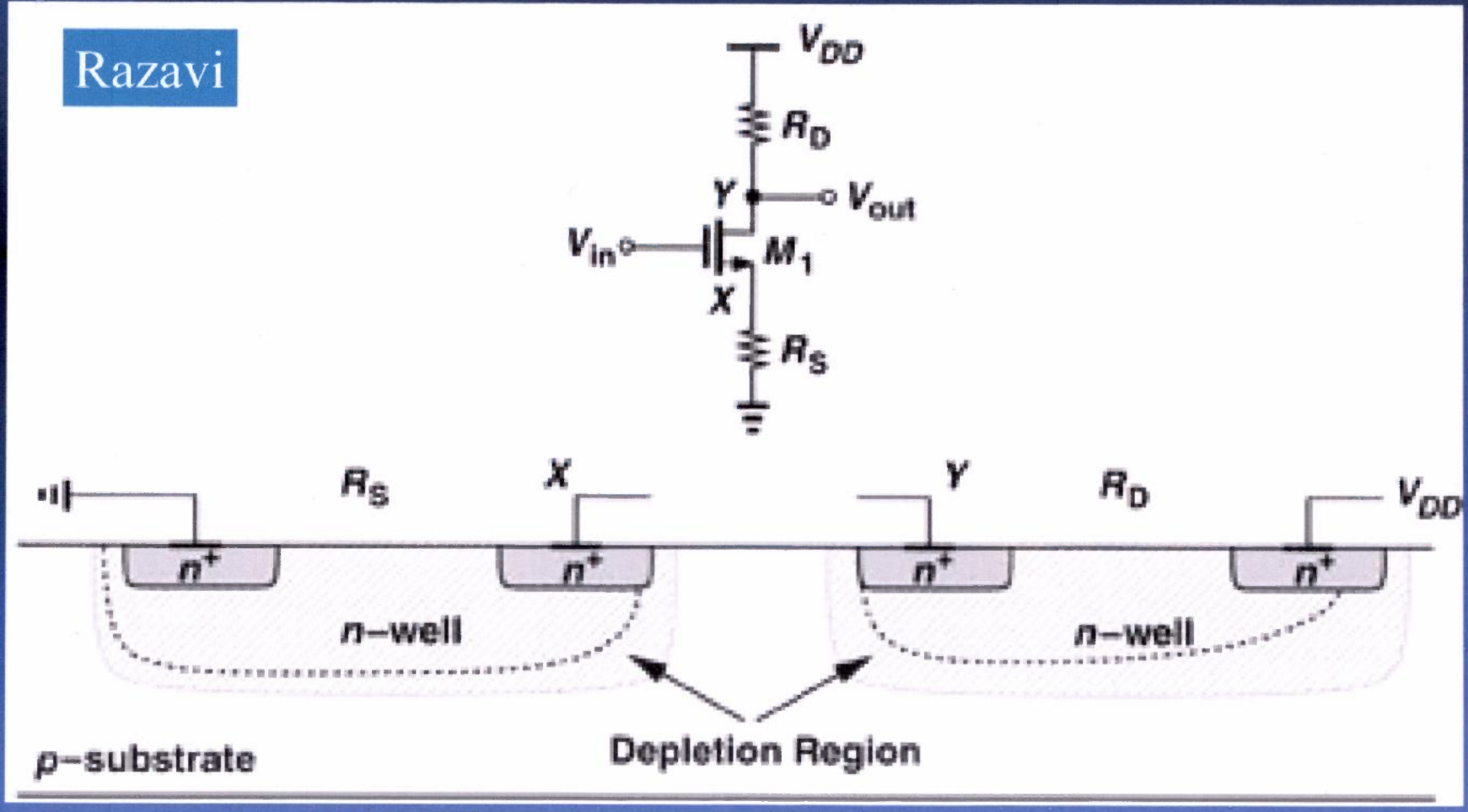
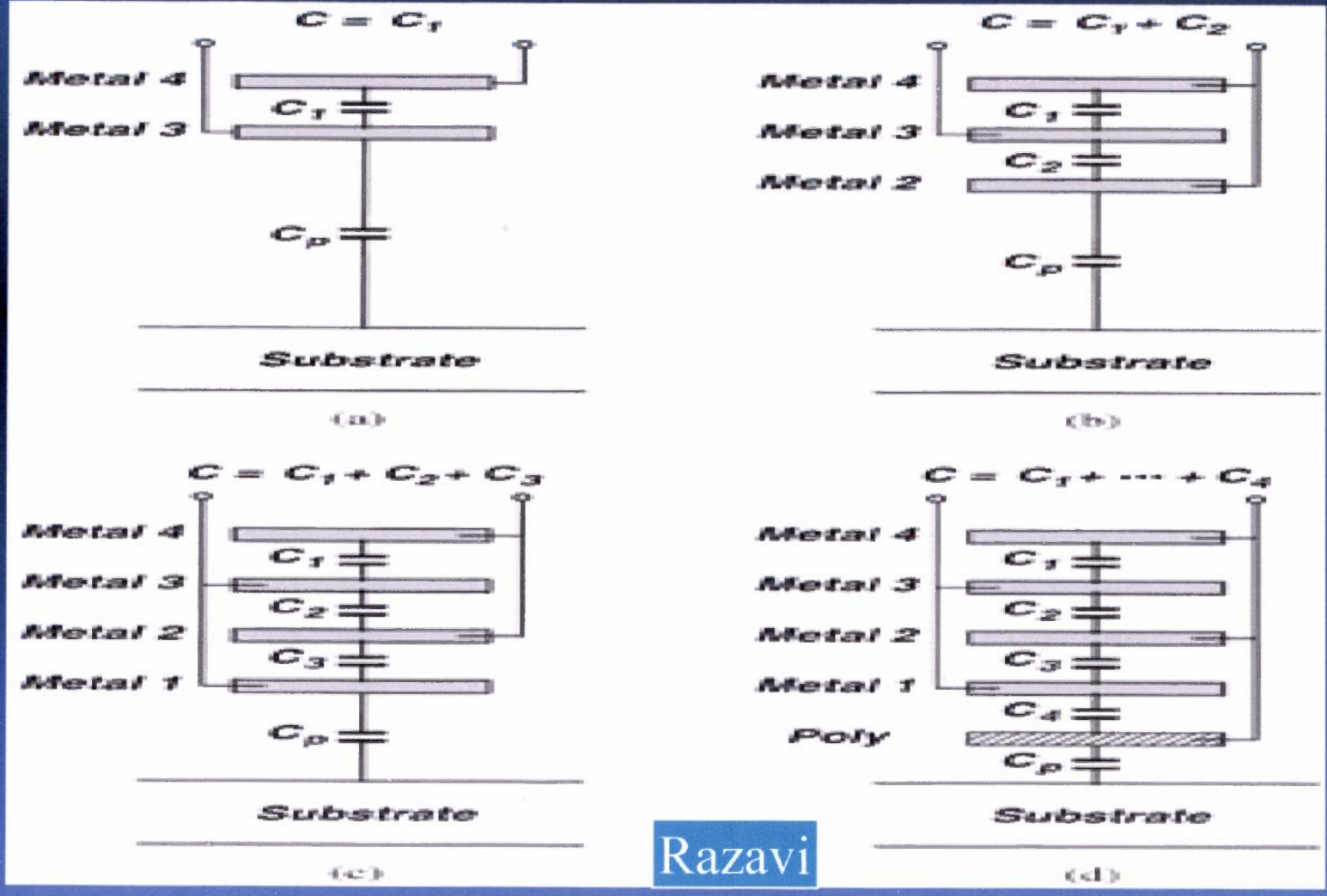


Capacitors



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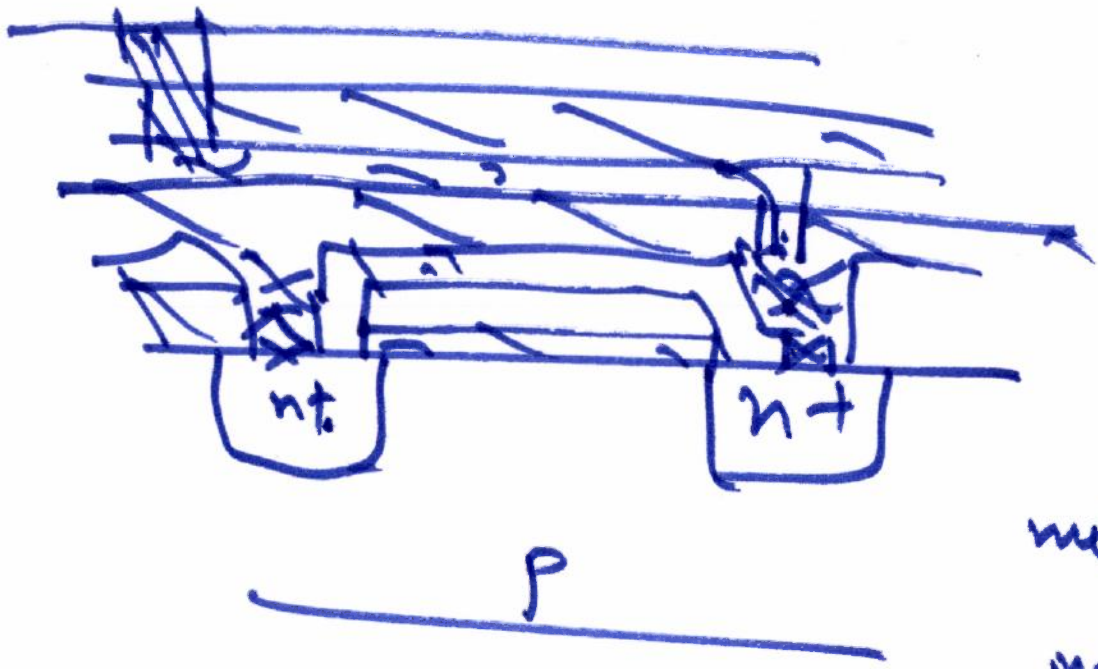
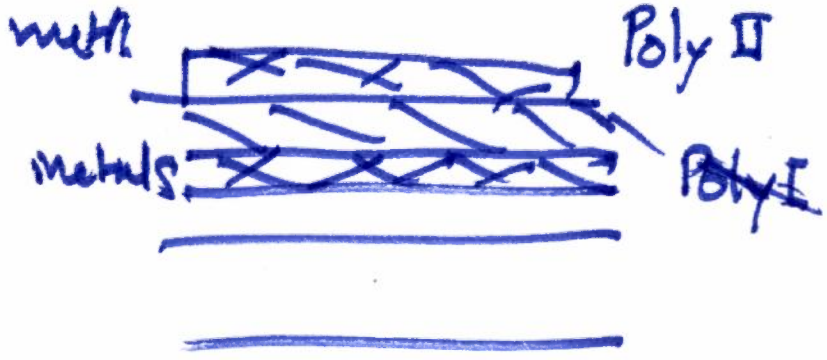
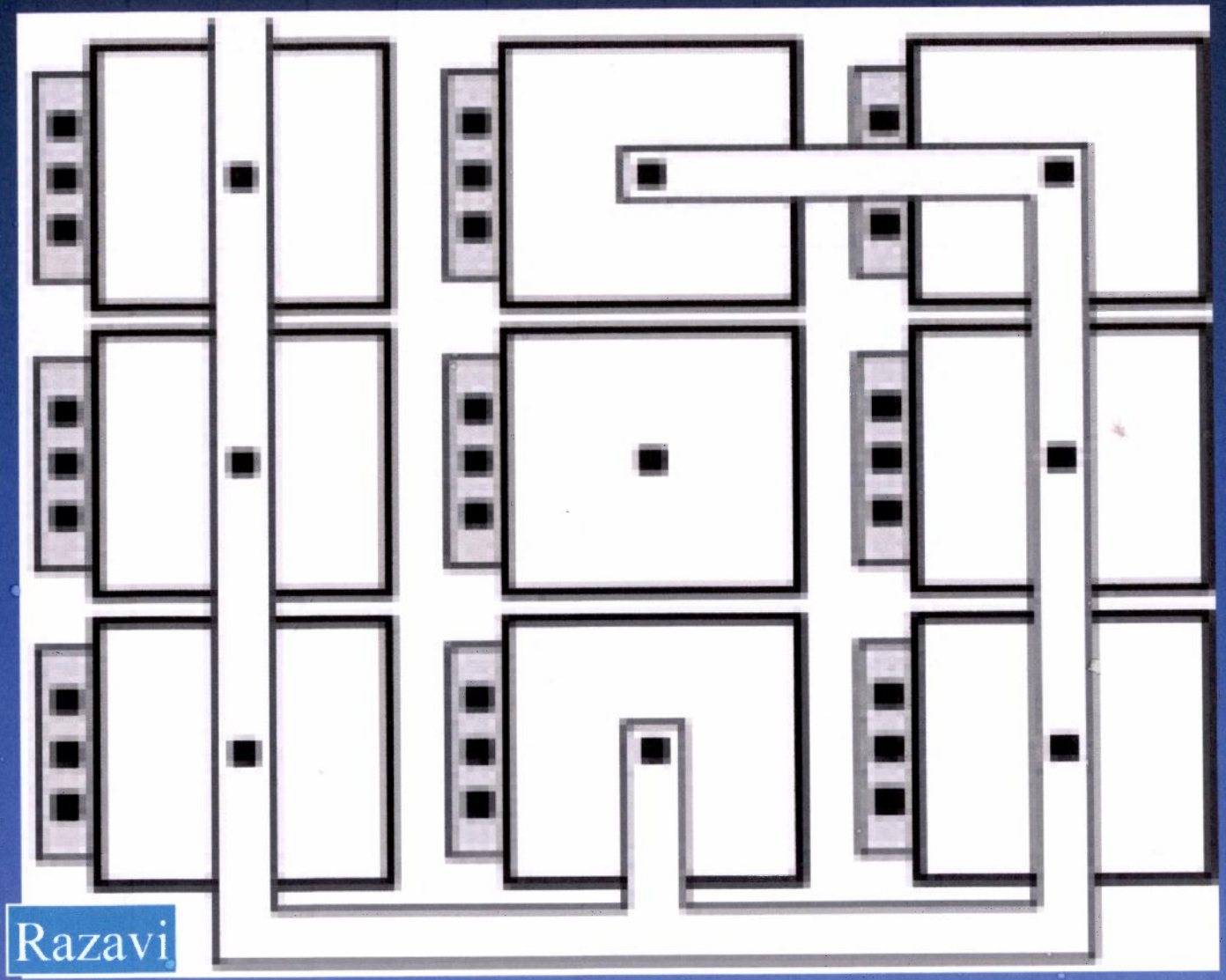

n+
n+
p


metal
Poly II
metal1
Poly I

Layout out of Interconnected capacitors



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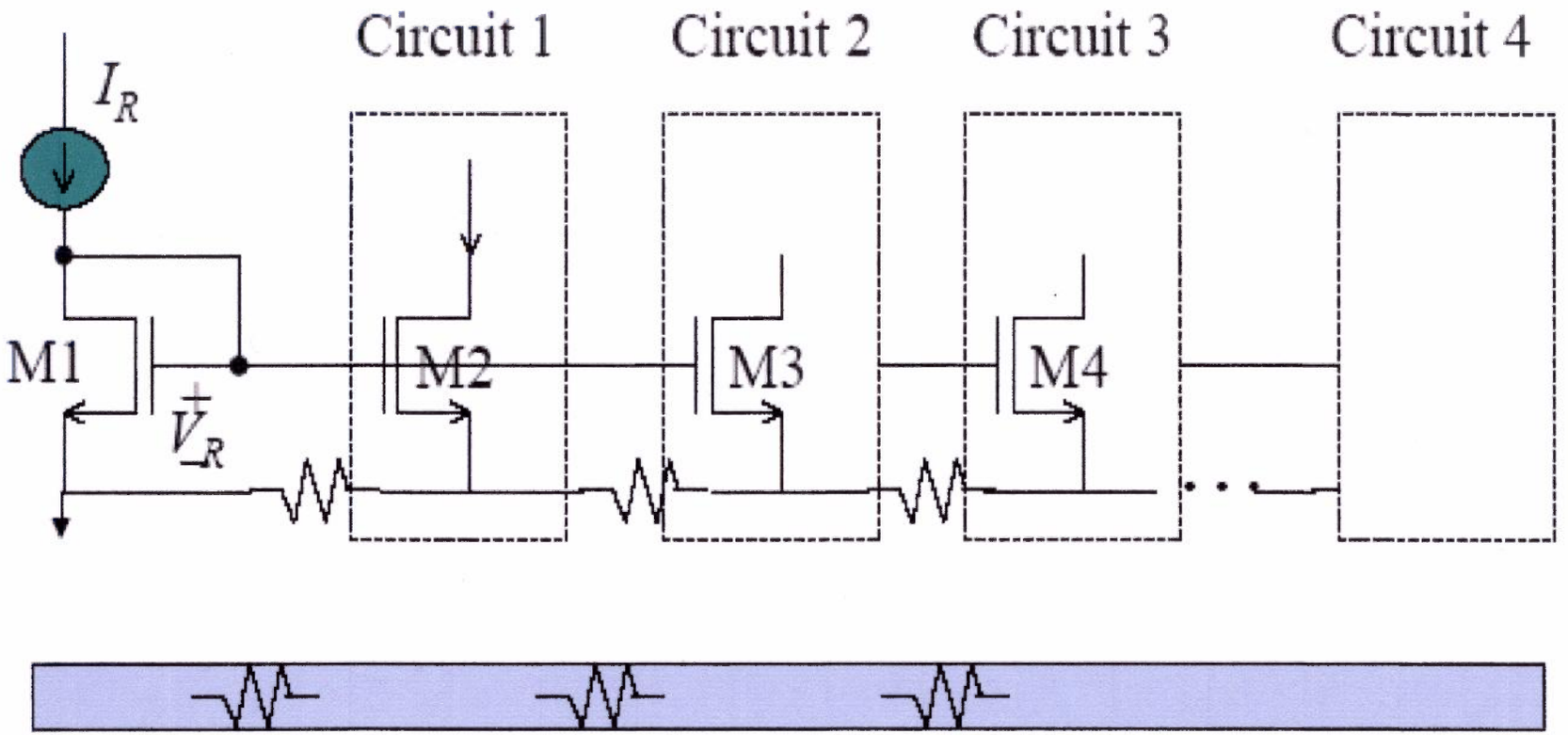
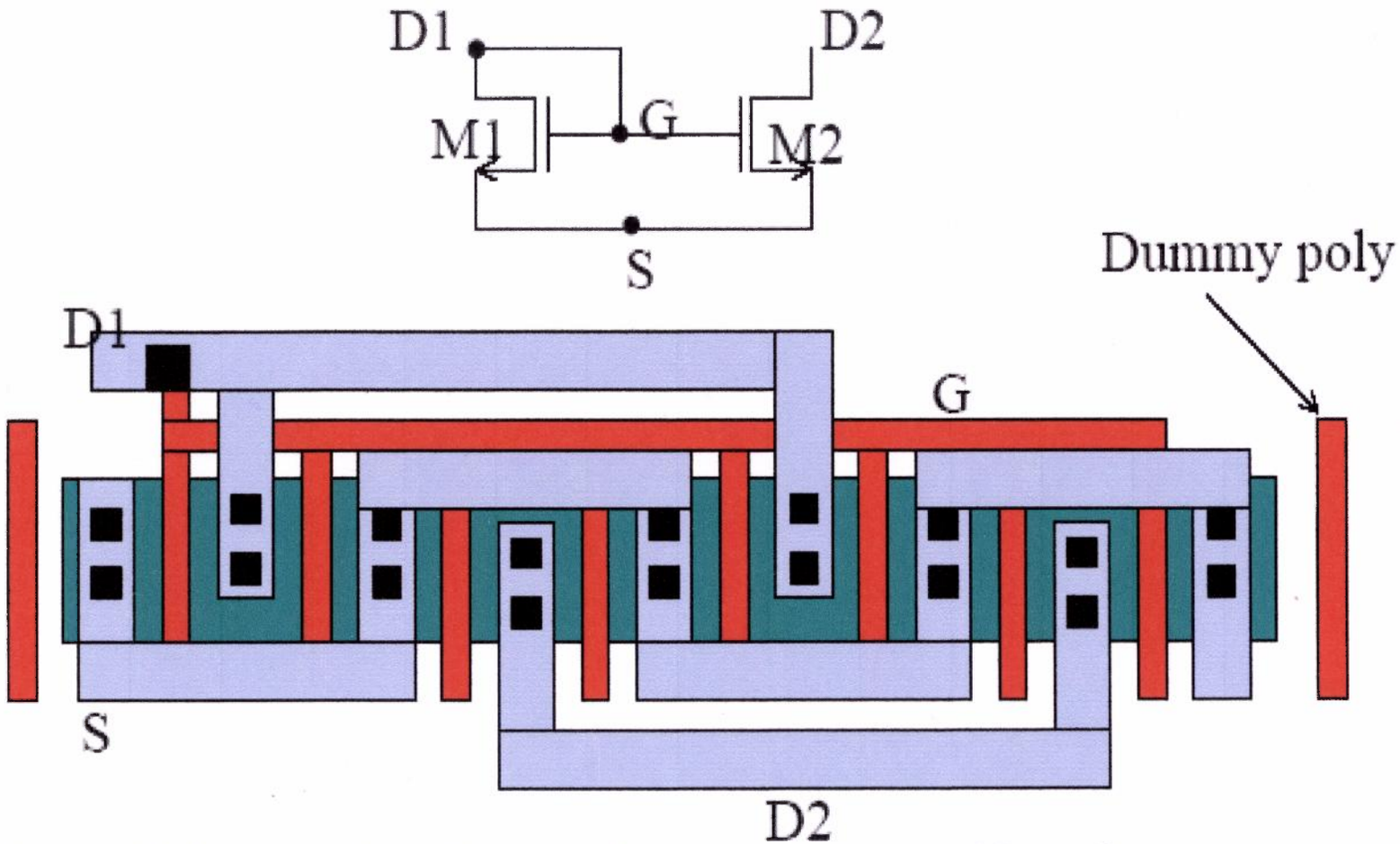
Interconnect routing



To distribute I_R in a large circuit, the resistance of ground bus makes $V_{gsn} \neq V_{gs1}$, thus affecting the current mirroring significantly

Interdigitation and dummy layer



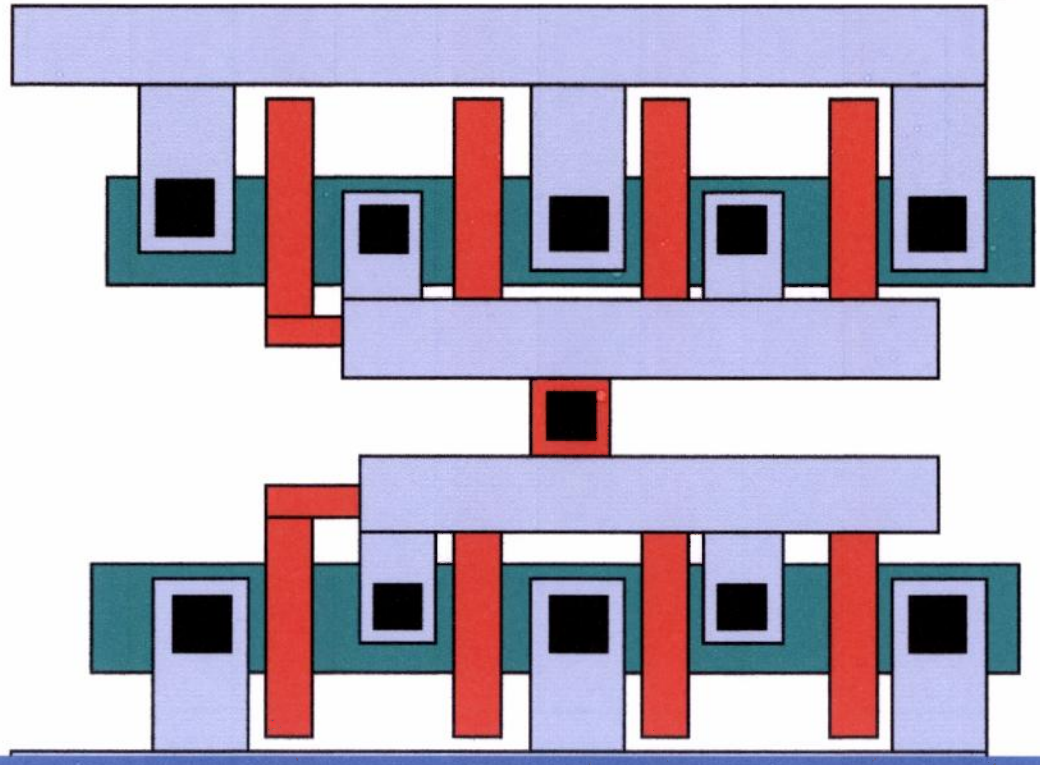
Interdigitation distributes the transistors uniformly

Dummy poly line eliminates loading effect in photo and etch

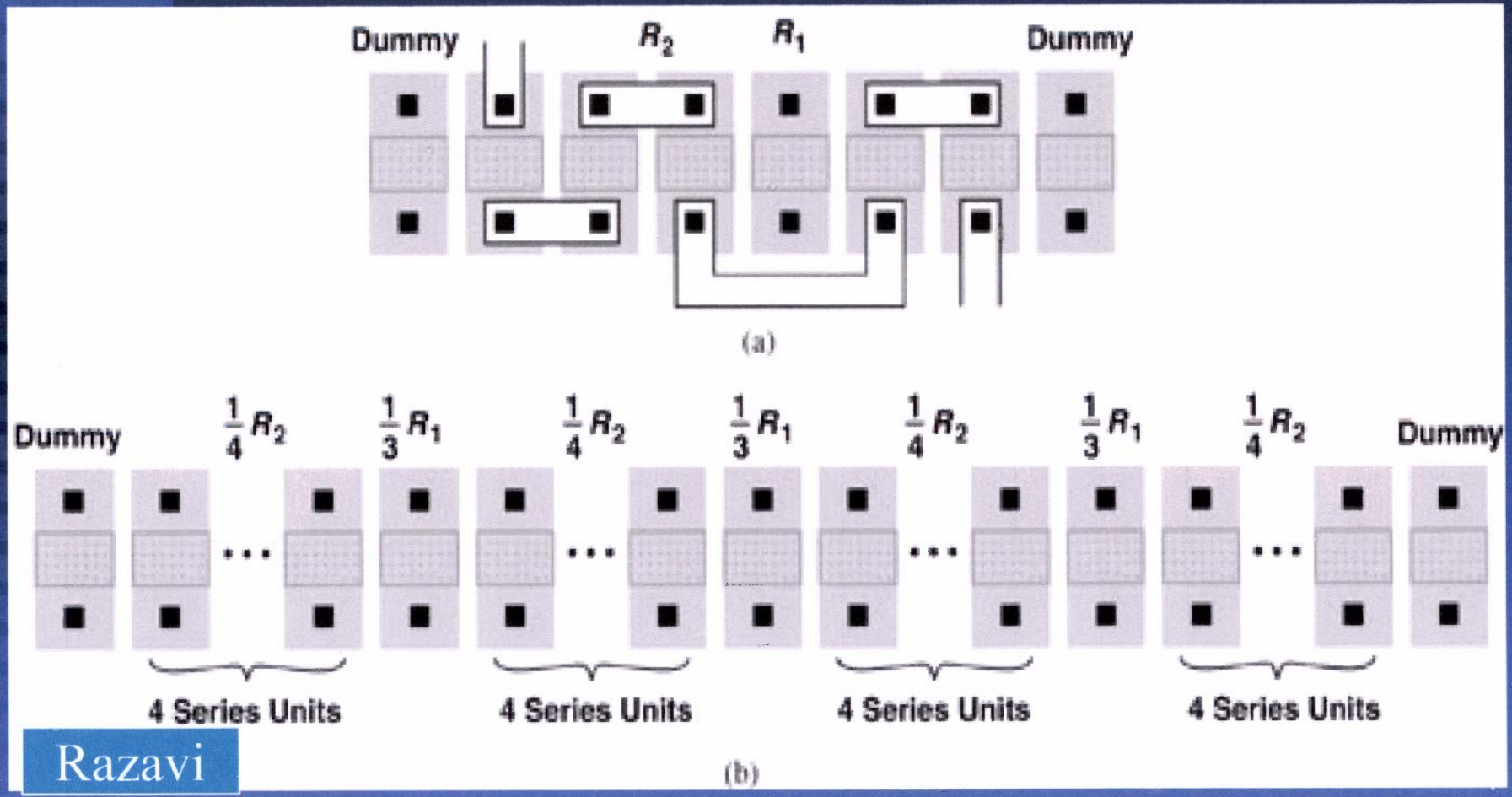
Unit cell repetition

Wide transistor should be laid out as parallel transistors of unit width to decrease gate resistance, s/d area capacitance as well as to counter ΔW effect

Disproportionate aspect ratio can be managed as below:



Layout of Resistances R2/R1=5



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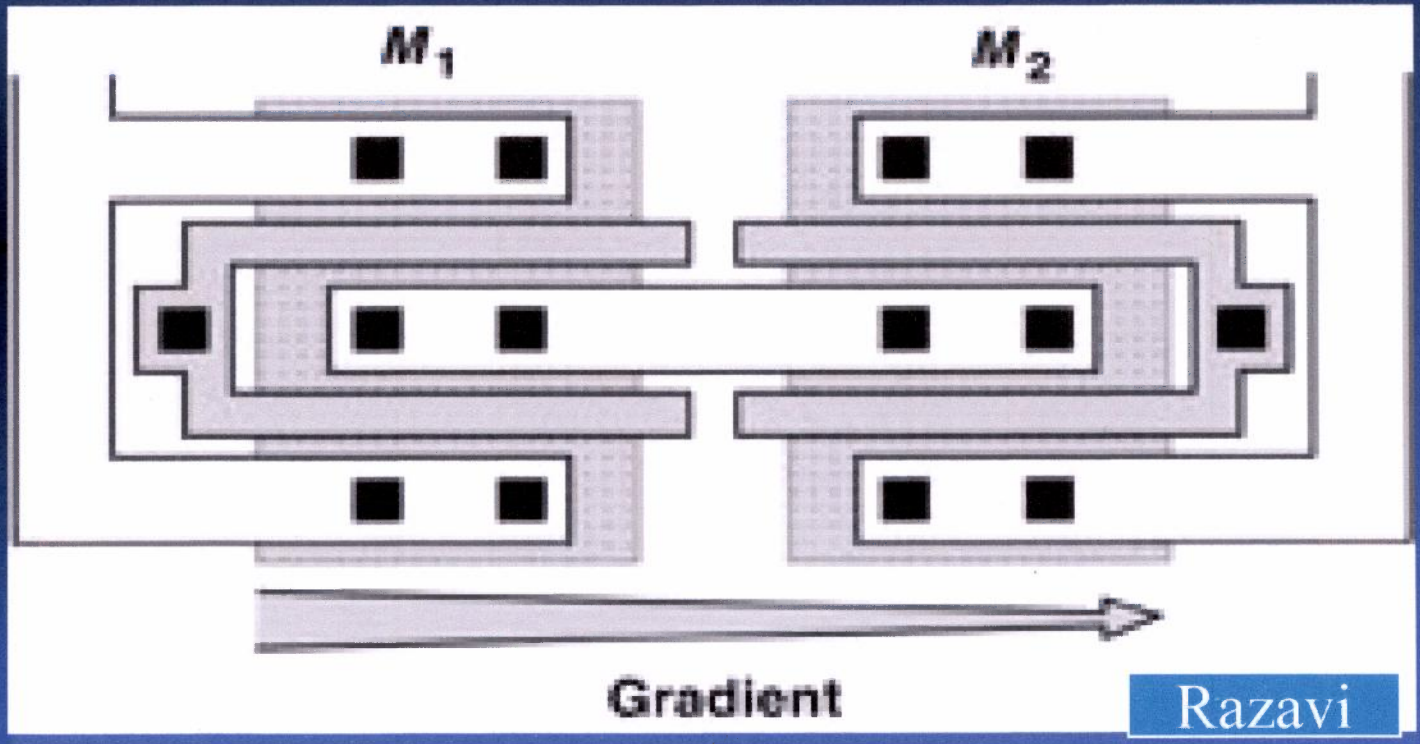
Gradient Effect



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Interconnect routing

Decrease the ground bus resistance

Provide multiple ground node connections if possible
And use short span ground bus

Keep several reference distributed in a large circuit
and mirror the reference locally