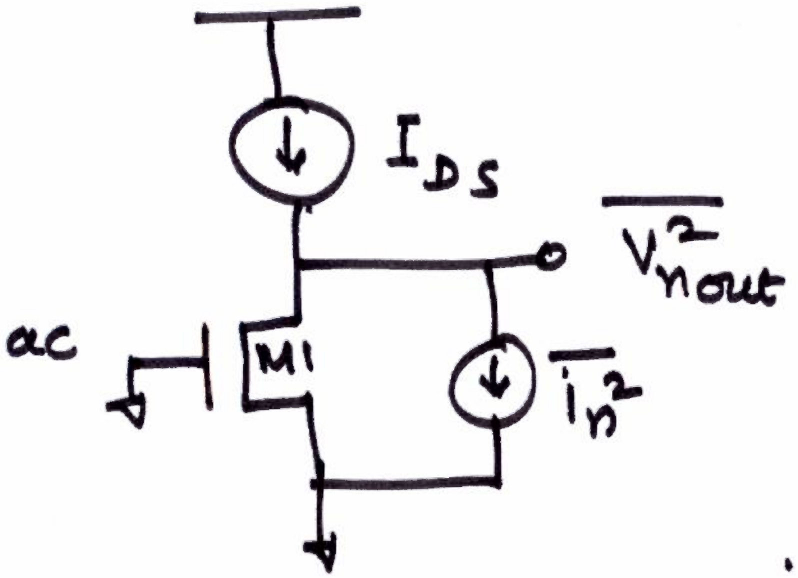
A simple CS Amplifier noise can be now evaluated.



If Rout is output resistance of M1 (r_{o1}) & Current Source has $R_{out} \to \infty$ Then Noise current $\sqrt{\overline{i_n^2}}$ flows through r_{o1} output resistance

$$\therefore \overline{V^2_{nout}} = \overline{i_n^2} \cdot r_{o1}^2$$

$$= 4kT\left(\frac{2}{3}g_m\right) r_{o1}^2$$

$$\text{or } \sqrt{\overline{V^2_{nout}}} = \sqrt{\frac{8}{3}kT g_m} \cdot r_{o1} \quad V/\sqrt{Hz}$$

$\therefore$ Low Noise $\Rightarrow$ low g_m. (Lower Gains)

$1/f$ Noise

- Famously known as Flicker Noise.
- Most Believe that this Noise is due to random carrier trapping at Interface States (Insulator / Semiconductor Interface) in MOS device.
- It is difficult to accurately predict the Noise Power due to $1/f$ Noise, as 'Interface' property is strongly dependent on Process Technology.
- This noise power is seen to follow $1/f$ relation with frequency f.

- In general one models this noise by Noise Voltage Source in series to Gate terminal.

CDEEP
IIT Bombay

- Typically it can be represented as

$$\overline{V^2_{n_{1/f}}} = \frac{K}{C_{ox} W \cdot L} \cdot \frac{1}{f}$$

&

$$\overline{i^2_{n_{1/f}}} = \frac{K}{C_{ox} W \cdot L} \cdot g_m^2 \cdot 1/f$$

- The spectral density of Flicker Noise current source is given by

$$\overline{i^2_{n_{1/f}}} = \int_{f_1}^{f_2} \frac{K_1}{L^2} \cdot \frac{I_{DS}}{C_{ox}} \frac{df}{f}$$

$$\overline{i^2_{n_{1/f}}} = \frac{K_1}{L^2} \frac{I_{DS}}{C_{ox}} \ln(f_2/f_1)$$

$$\overline{i^2_{n_{1/f}}} = \frac{K_2}{L^2} \frac{I_{DS}}{C_{ox}} \log(f_2/f_1)$$

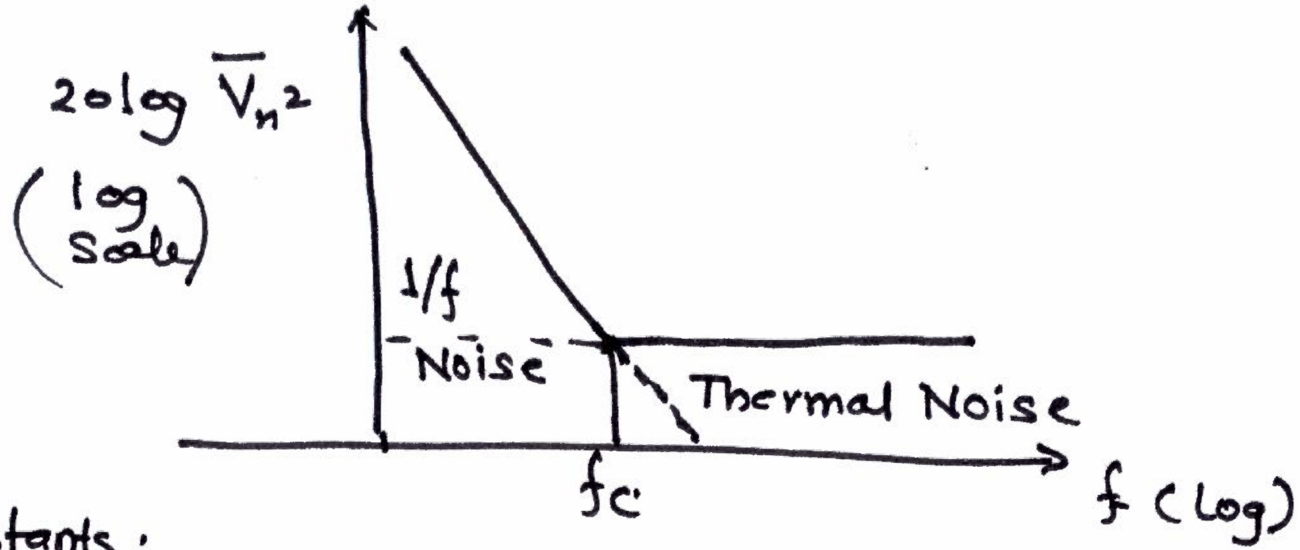
We also know that Thermal Noise ~~Voltage~~ current in a frequency band can be written as

$$\overline{i^2_{n_{th}}} = 4kT\left(\frac{2}{3} g_m\right)$$

At a frequency f_c called <u>1/f Noise Corner frequency</u> the two noise voltages are equal

or $$4kT\left(\frac{2}{3} g_m\right) = \frac{K}{C_{ox} W \cdot L} \cdot \frac{1}{f_c} g_m^2$$

or $$f_c = \frac{K g_m}{C_{ox} W \cdot L} \frac{3}{8kT}$$



Constants :

$K_{1\,NMOS} = 2\times10^{-29}$ A.F
$K_{1\,PMOS} = 3.5\times10^{-30}$ A.F
] 0.25 μ

$K = 1.06\times10^{-25}$ V^2.F (90 nm Tech.)

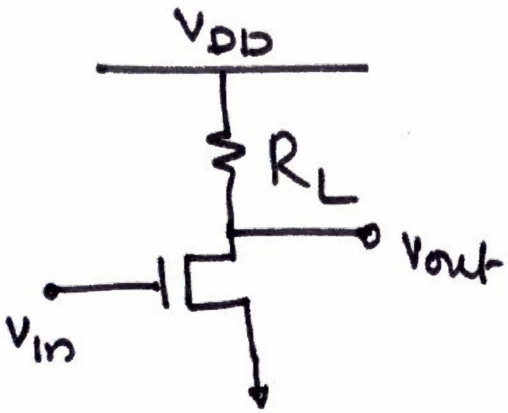
CDEEP
IIT Bombay

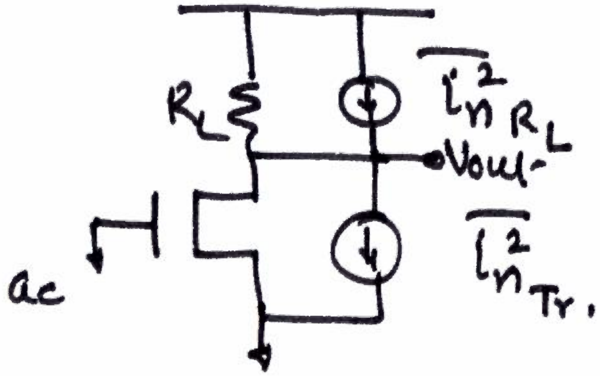
(i) As K_1 values are larger for NMOS Devices compared to PMOS devices, f_c for NMOS Devices is larger than that for PMOS devices.

(ii) Further $f_c \propto \frac{1}{L^2}$ i.e. f_c increases with Technology Scaling.

(iii) Finally $f_c \propto \frac{1}{g_m/I_{DS}}$, gives understanding that larger g_m devices reduces f_c, meaning $1/f$ noise dominates over thermal noise

Noise in CS Amplifier





$$\overline{i_n^2}_{R_L} = \frac{4kT}{R_L}$$

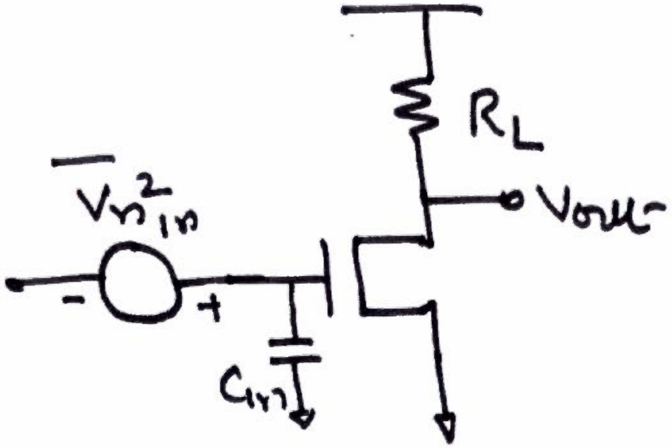
$$\therefore \overline{V_{n_{out}}^2} = \left[4kT\,\frac{2}{3}g_m + \frac{K}{C_{ox}W\cdot L}\cdot\frac{1}{f}g_m^2 + \frac{4kT}{R_L}\right]R_L^2$$

Input Refered Noise

$$\overline{V_{n_{in}}^2} = \overline{V_{n_{out}}^2} / A_{vo}^2 \quad , \quad A_{vo} = -g_m R_L$$

$$= \left[4kT\left(\frac{2}{3}g_m\right) + \frac{K}{C_{ox}W\cdot L}\cdot\frac{g_m^2}{f} + \frac{4kT}{R_L}\right]\frac{R_L^2}{g_m^2 R_L^2}$$

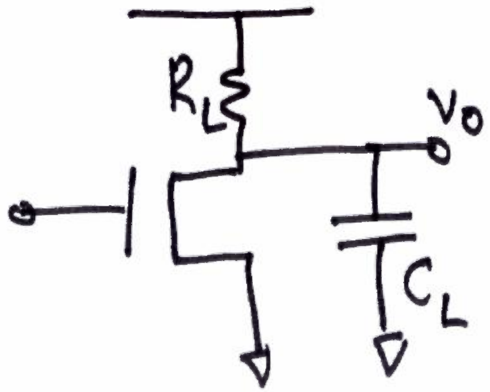
or $$\overline{V^2_{n_{in}}} = \frac{8}{3}\frac{kT}{g_m} + \frac{K}{C_{ox}WL}\cdot\frac{1}{f} + \frac{4kT}{g_m^2 R_L}$$



∴ For CS Amplifier

$$\overline{V^2_{n_{in}}} = 4kT\left(\frac{2}{3g_m} + \frac{1}{g_m^2 R_L}\right) + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}$$

gives Input Referred Noise.



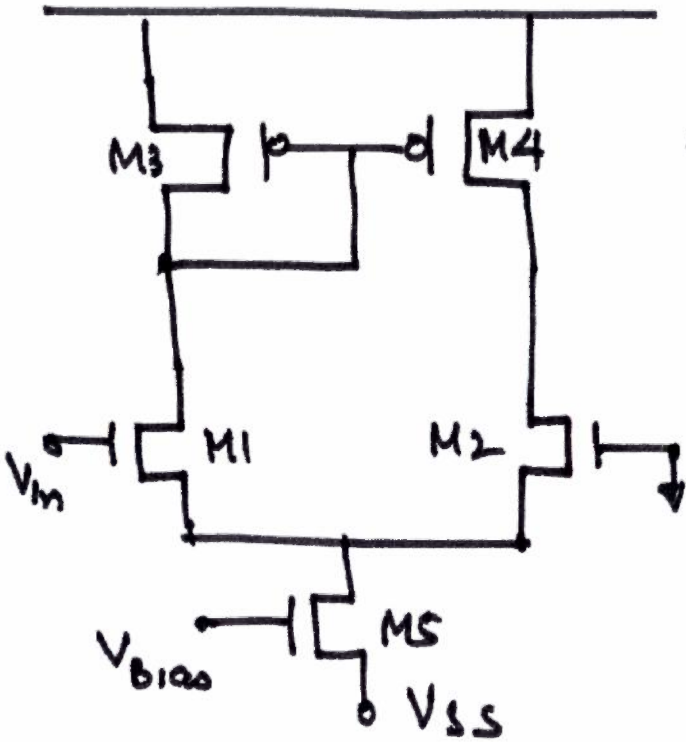
$$\overline{V^2_{n_{out}}} = \left[\frac{8}{3}kTg_m + \frac{4kT}{R_L}\right]\left|\frac{R_L}{1+j\omega R_L C_L}\right|^2 df$$

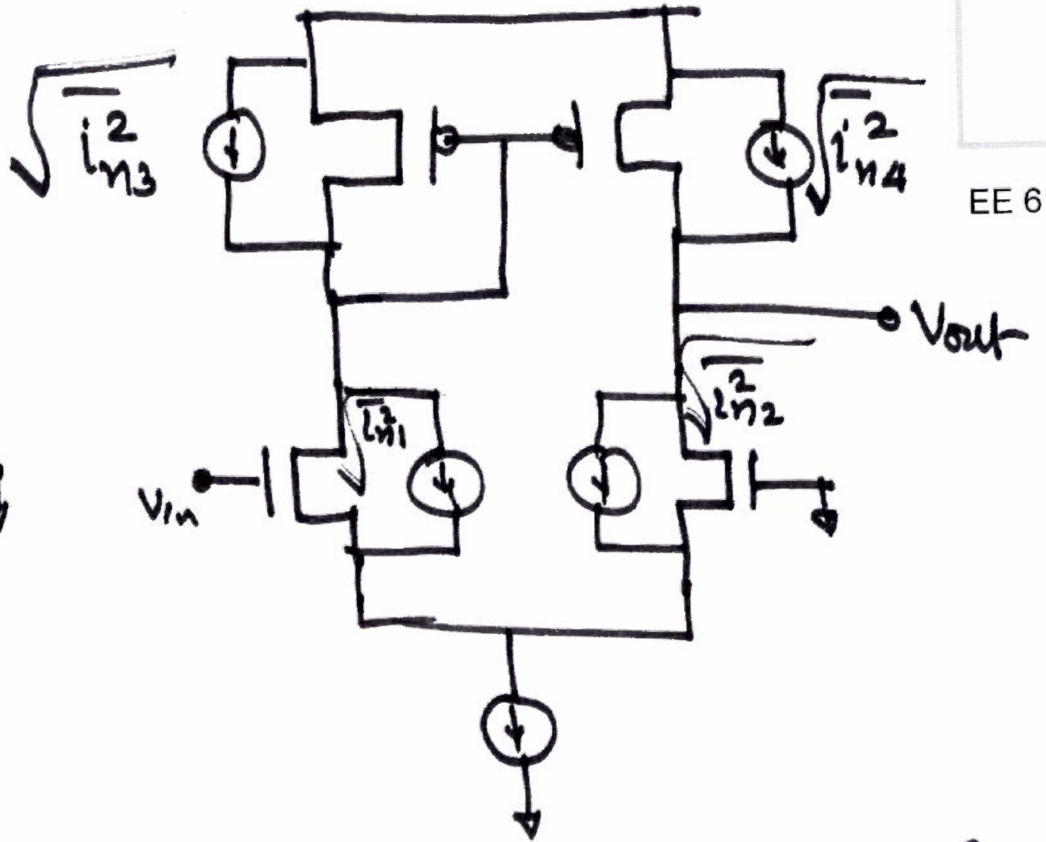
$\omega > f_c$ is assumed

$$\therefore \overline{V^2_{n_{out}}} = \int_0^{\infty} 4kT\left(\frac{1}{R_L} + \frac{2}{3}g_m\right)\left|\frac{R_L}{1+j\omega R_L C_L}\right|^2 df$$

$$= \frac{kT}{C_L}\left(1 + g_m\cdot\frac{2}{3}R_L\right) \simeq \frac{kT}{C}\left(1 + |A_{vo}|\right)$$

Noise in DIFFAMP





$$\overline{i_n^2} = 4kT\left(\frac{2}{3}g_m\right) + \frac{K}{C_{ox}W\cdot L}\frac{g_m^2}{f} \quad A^2/Hz$$

$$\overline{i^2_{nout}} = \overline{i^2_{n1}} + \overline{i^2_{n2}} + \overline{i^2_{n3}} + \overline{i^2_{n4}}$$

$$\overline{V^2_{total\,n\,out}} = \overline{i^2_{n\,out}} \cdot (r_{o2} \| r_{o4})^2 \qquad V^2/Hz$$

$$\therefore \overline{V^2_{T n_{MR}}} = \frac{V^2_{Total\,n\,out}}{A_{V0}^2} = \frac{1}{g^2_{m1}(r_{o2}\|r_{o4})^2} \cdot \overline{V^2_{Total\,n\,out}}$$

$$\therefore \overline{V^2_{T n_{MR}}} = \frac{\overline{i^2_{n\,out}} \cdot (r_{o2}\|r_{o4})^2}{g^2_{m1}\,(r_{o2}\|r_{o4})^2}$$

$$= \frac{\overline{i^2_{n\,out}}}{g^2_{m1}}$$

$$\overline{i^2_{n\,out}} = 4kT\left(\tfrac{2}{3}g_{m1}\right) + \frac{K}{C_{ox}W_1L_1}\cdot\frac{g^2_{m1}}{f} + 4kT\left(\tfrac{2}{3}g_{m2}\right) + \frac{K}{C_{ox}W_2L_2}\frac{g^2_{m2}}{f} + 4kT\left(\tfrac{2}{3}g_{m3}\right) + \frac{K}{C_{ox}W_3L_3}\cdot\frac{g^2_{m3}}{f} + 4kT\left(\tfrac{2}{3}g_{m4}\right) + \frac{K}{C_{ox}W_4L_4}\cdot\frac{g^2_{m4}}{f}$$

$$g_{m1} = g_{m2} \quad , \quad \frac{W_1}{L_1} = \frac{W_2}{L_2}$$

$$g_{m3} = g_{m4} \quad ; \quad \left(\frac{W}{L}\right)_3 = (W/L)_4$$

$$\therefore \overline{i^2_{nout}} = 8kT\left(\frac{2}{3}g_{m1}\right) + \frac{2K g_{m1}^2}{f} \cdot \frac{1}{C_{ox} W_1 L_1}$$

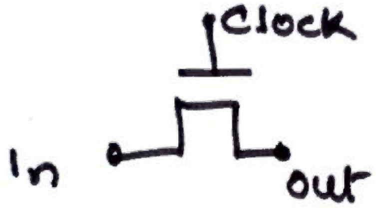
$$+ 8kT\left(\frac{2}{3}g_{m3}\right) + \frac{2K g_{m3}^2}{f} \cdot \frac{1}{C_{ox} W_3 \cdot L_3}$$

$$\therefore \overline{V^2_{Tn_{INR}}} = \frac{16kT}{3g_{m1}} + \frac{2K}{C_{ox} W_1 L_1} \cdot \frac{1}{f}$$

$$+ \frac{16kT}{3} \cdot \frac{g_{m3}}{g_{m1}^2} + 2K\left(\frac{g_{m3}}{g_{m1}}\right)^2 \cdot \frac{1}{C_{ox} W_3 L_3} \cdot \frac{1}{f}$$

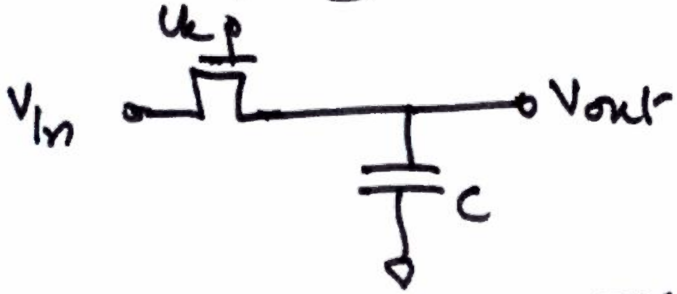
CDEEP
IIT Bombay

In Sampling Mode, the MOS Transistor is used as Switch. Switch is characterised as



=>

In sampling we have circuit like shown. When Switch is 'ON', C charges to $V_{in} = V_{out}$ and when Switch is 'OFF', last V_{out} is retained or 'hold'.



This RC circuit gives $\frac{kT}{C}$ noise.

For such a circuit

$$SNR = \frac{P_{av}}{P_{noise}} = \frac{\frac{1}{2}\overline{V_{out}^2}}{\frac{kT}{C}} \propto C\,\overline{V_{out}^2} \text{ at a Temp.}$$

SNR obtained is around 80 db.