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A Two Stage Single Ended

OPAMP DESIGN

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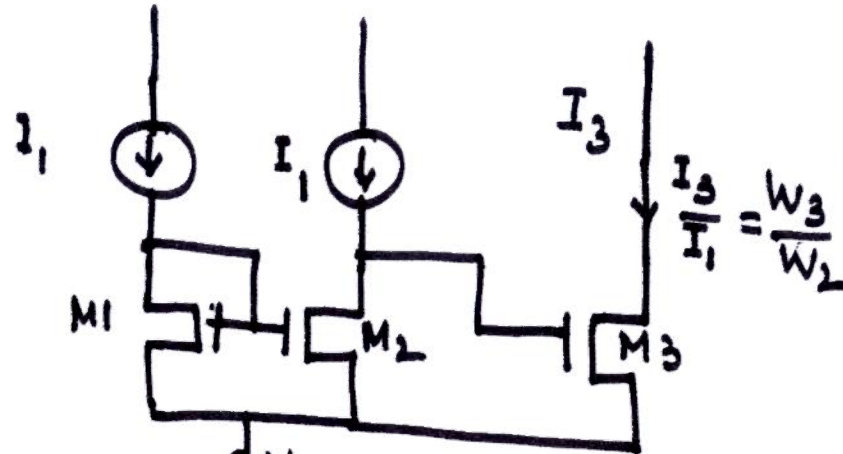
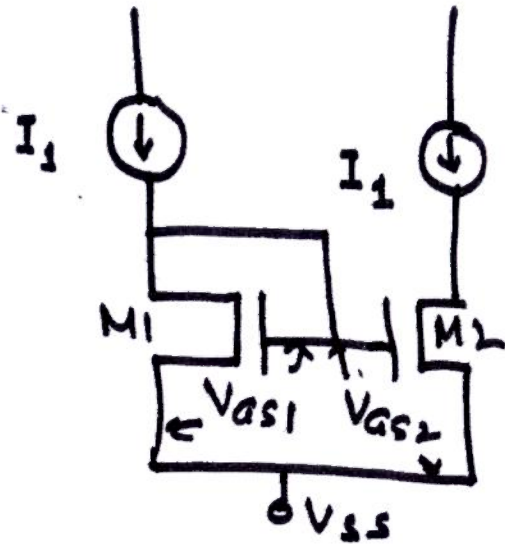
Other OPAMP structures (cascode type)

Proof for  $V_{GS3} = V_{GS4} = V_{GS6}$  in OPAMP



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Normal Current Mirror ← CS Amplifier →

Current Mirror: If  $I_{DS2} = I_{DS1}$   
when  $W_1 = W_2$  &  $V_T$  is same for both.

$$V_{GS1} = V_{GS2}$$

$$V_{GS1} = V_{DS1}$$

$$\therefore V_{GS2} = V_{DS1}$$

$$\text{and } V_{DS1} = V_{DS2}$$

Since  $V_{GS1} = V_{GS2} = V_{DS2}$

Hence if  $D_2$  ( $V_{DS2}$ ) is connected to  $G_3$ , then

$$V_{GS3} = V_{DS2} = V_{GS1} = V_{GS2}$$

$$\therefore I_3 = \beta_n' \left(\frac{W}{L}\right)_3 (V_{GS3} - V_T)^2$$

$$I_2 = \beta_n' \left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2$$

$$\therefore \frac{I_3}{I_2} = \frac{I_3}{I_1} = \frac{(W/L)_3}{(W/L)_2}$$

## Other OPAMPS

1. CASCODE OPAMP
2. High Performance OPAMP
3. High-Speed OPAMP
4. Differential Output OPAMP
5. Micropower OPAMP
6. Low Noise OPAMP
7. Chopper Stabilised OPAMP
8. Low-Voltage OPAMP



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## ① Single Stage CASCODE OPAMP

To improve Stability Issues, one possibility that we have single stage OPAMP (DIFFAMP)

with larger Gain. Since there is no second stage, 'second pole' will not exist. Thus increasing the Stability. To improve the Gain, we can have CASCODE DIFFAMP.

CASCODE STAGE improves  $R_{out}$  and hence we can get higher Gain  $g_m R_{out} = A_{vo}$ . Then

$$\text{Bandwidth} = \frac{GBW}{A_{vo}} = \text{Dominant Pole} = \frac{1}{R_{out}C_{out}}$$



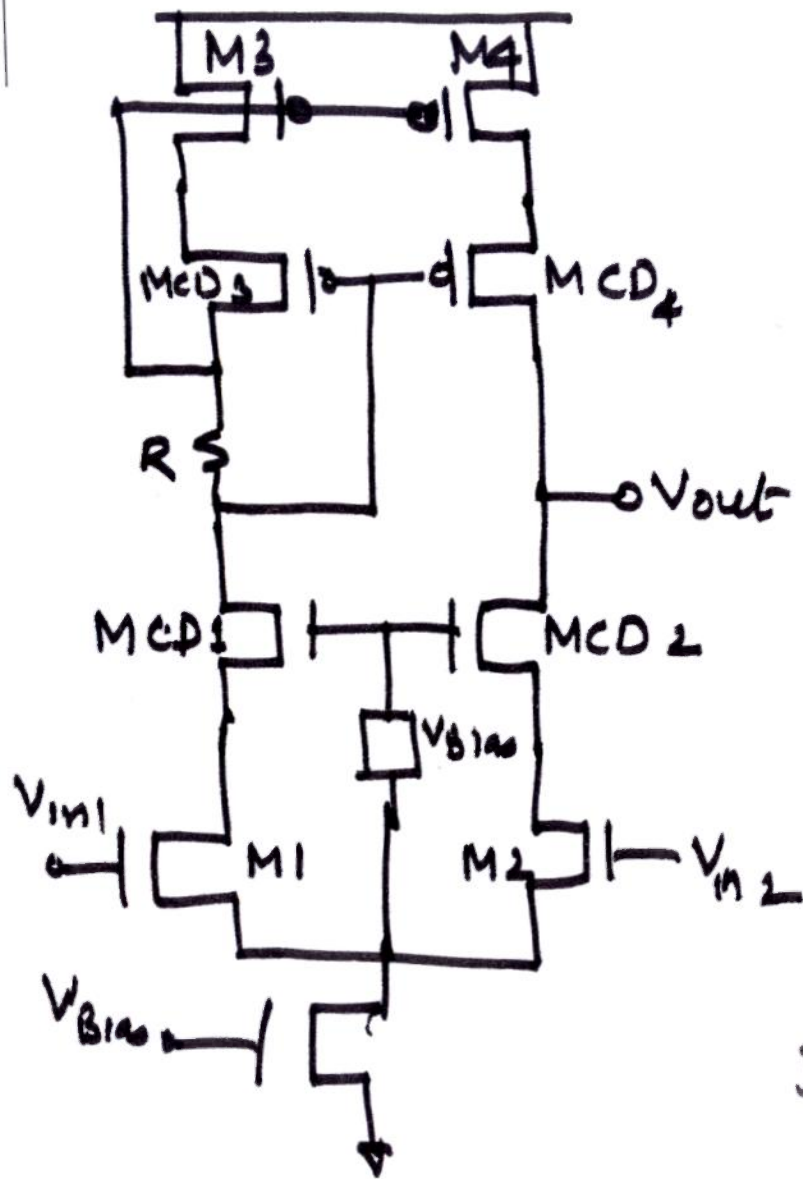
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$MCD_1$  to  $MCD_4$  gives  
cascode configuration  
 $R$  provides  $V_{as}$  for  $MCD_3$   
and allows mirror to  
 $MCD_4$ .

$V_{Bias}$  provides bias for  $MCD_1$   
and  $MCD_2$  and thus fixes  
 $V_{DS}$  for  $M1$  &  $M2$  close to  
 $V_{DSat,1} = V_{DSat,2}$

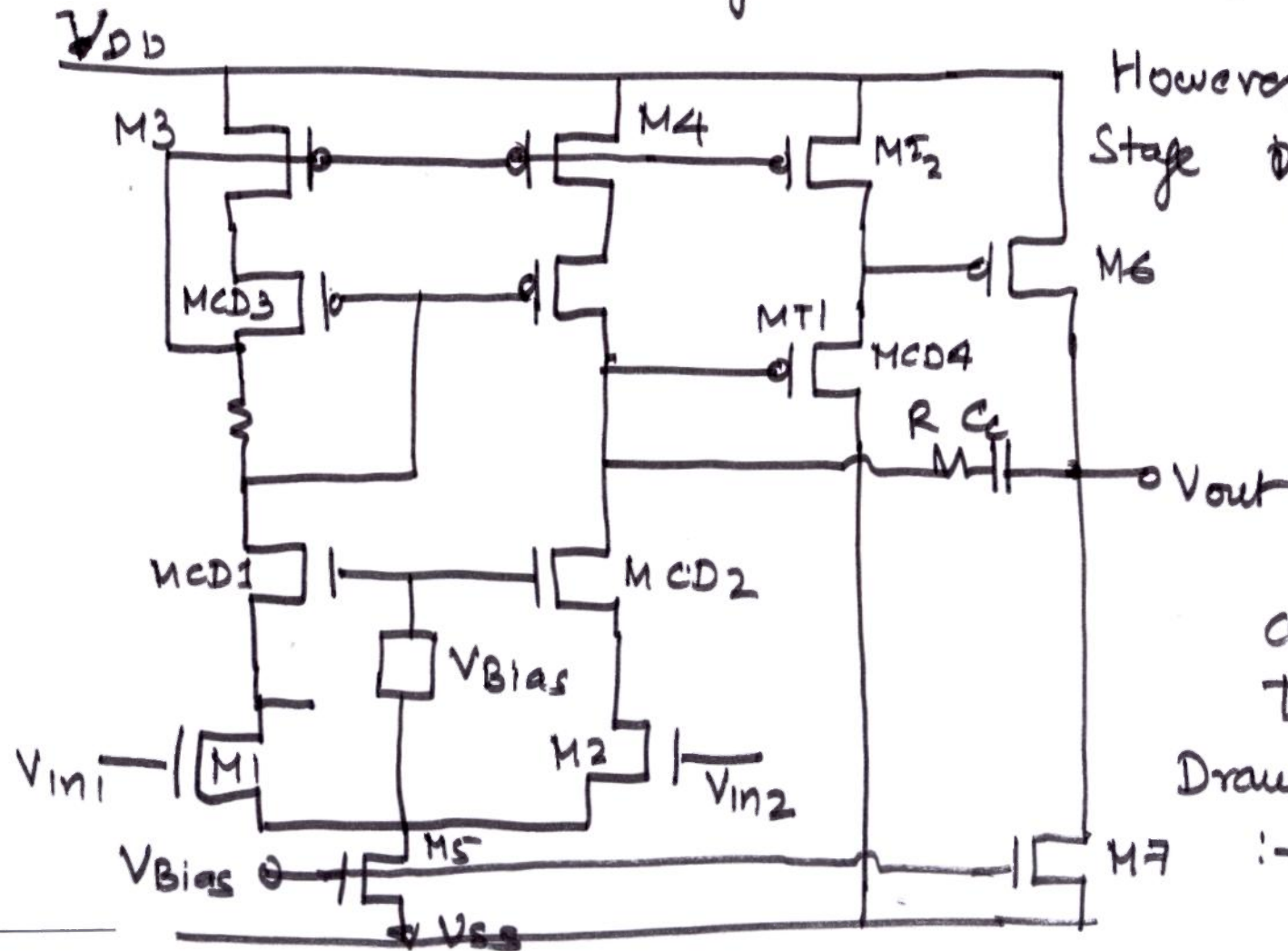
Drawback : Reduced ICNR &  $V_{oswing}$



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Single stage Cascode OPAMP with cascode in Diffamp stage can be improved by putting cascode at second stage (CS Amplifier) @  $V_{DD}$



However the Single Cascode Stage Output is to be given to Buffer Stage which we shall see later.

MT1 & MT2

are called level translator,

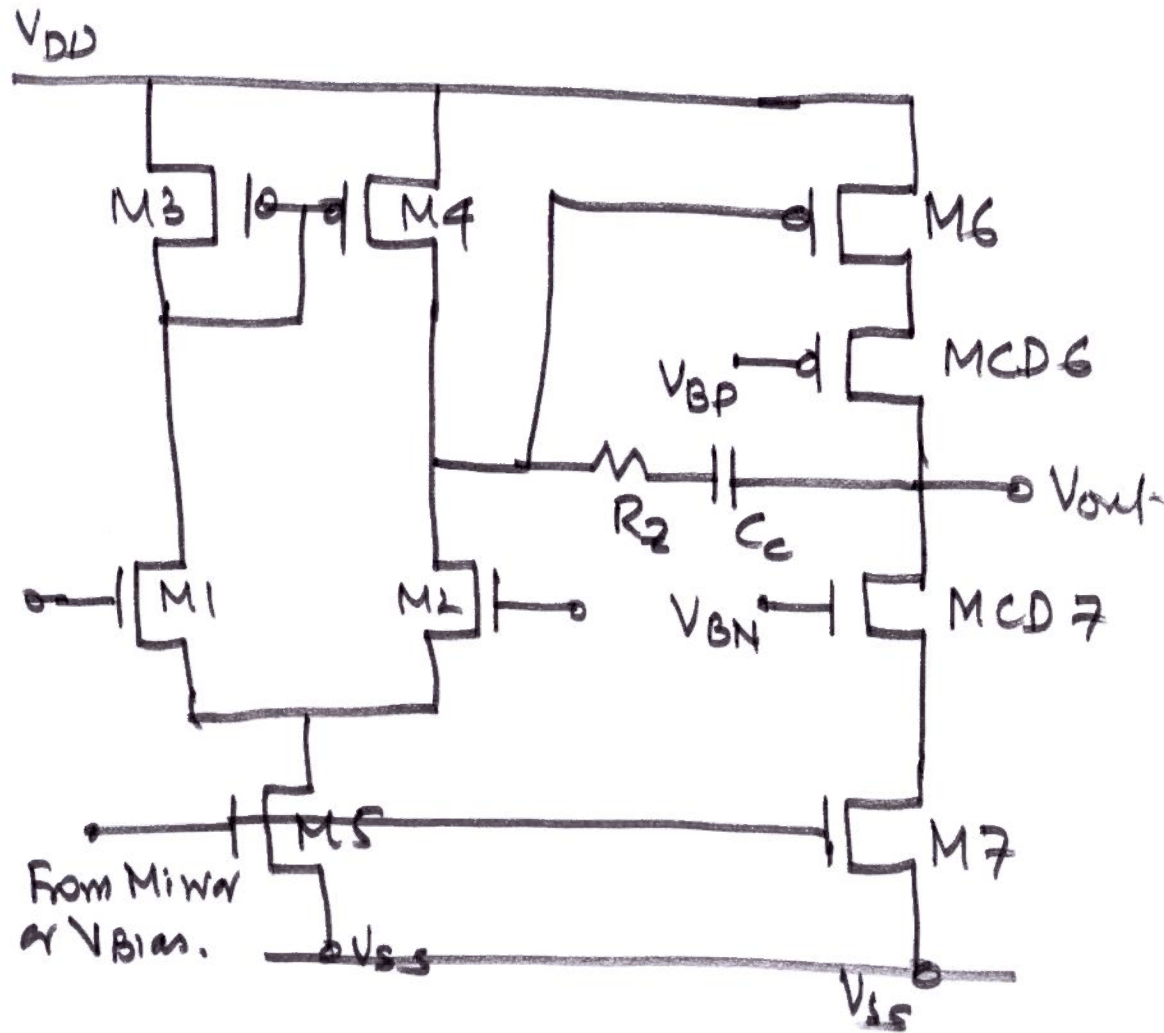
Drawback without MT1 & MT2 :-



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CASCODE only at Output Stage (CS stage)  
in an OPAMP



$$A_{V0} = A_{V01} \cdot A_{V02}$$

$$A_{V02} = -g_{m1} (r_{o2} \parallel r_{o4})$$

$$\begin{aligned} A_{V02} &= -g_{m2} (R'_{o6} \parallel R'_{o7}) \\ &= -g_{m2} R_{out} \end{aligned}$$

$$\begin{aligned} R_{out} &= (g_{m_{CD6}} \cdot r_{o6} \cdot r_{oc}) \\ &\parallel (g_{m_{CD7}} \cdot r_{o7} \cdot r_{oc7}) \end{aligned}$$

An OPAMP always has a Buffer Stage as Output Amplifier.



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The Output Amplifier is necessary as output capacitive load may be large and often not exactly known. Hence Slew Rate at the output load can only be improved if Driving current (Sinking current) is large and not governed by Second Stage Amplifier requirements.

Typically an AB or B-type Amplifier can be used as an Output Amplifier.

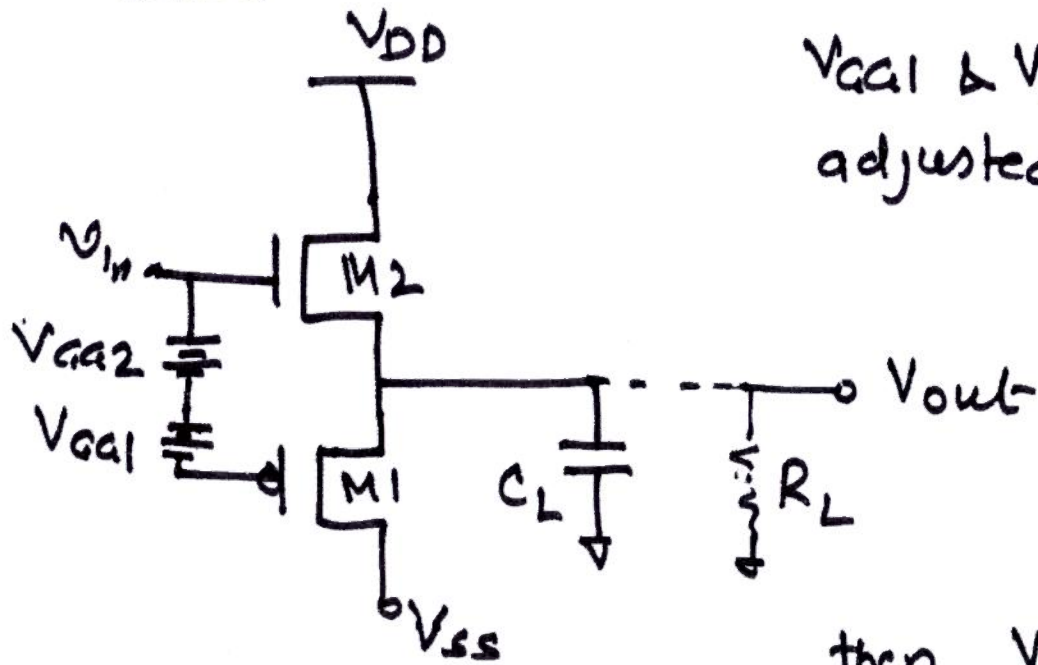


A typical Class B or AB Amplifier basics could be understood by using circuit below



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$V_{GA1}$  &  $V_{GA2}$  are so adjusted that the Amplifier can be Class - A  
Class - B  
or Class - AB Type

If  $V_m$  (moderately large) increases then  $V_{GS2}$  increases  $\Rightarrow$  Current in M2 Increases

And Also  $V_{GS1}$  decreases  $\Rightarrow$  Current in M1 Decreases

When  $V_{in}$  is large enough (+tive), M1 can turn-off, and then current in M2 charges  $C_L$ . Since current in M2 is not connected to currents in earlier CS stage, hence SR could be larger.



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By same argument,  $M_1$  can be fully on with  $M_2$  OFF, for  $V_{in}$  -ve and large. Thus  $C_L$  can discharge through  $M_1$ .

For some value-band of  $V_{in}$ , both  $M_1$  &  $M_2$  will be ON. This is what we say, the Amplifier working in class AB.

The output voltage swing will be then

$$V_{omax} = V_{DD} - V_{TN}$$

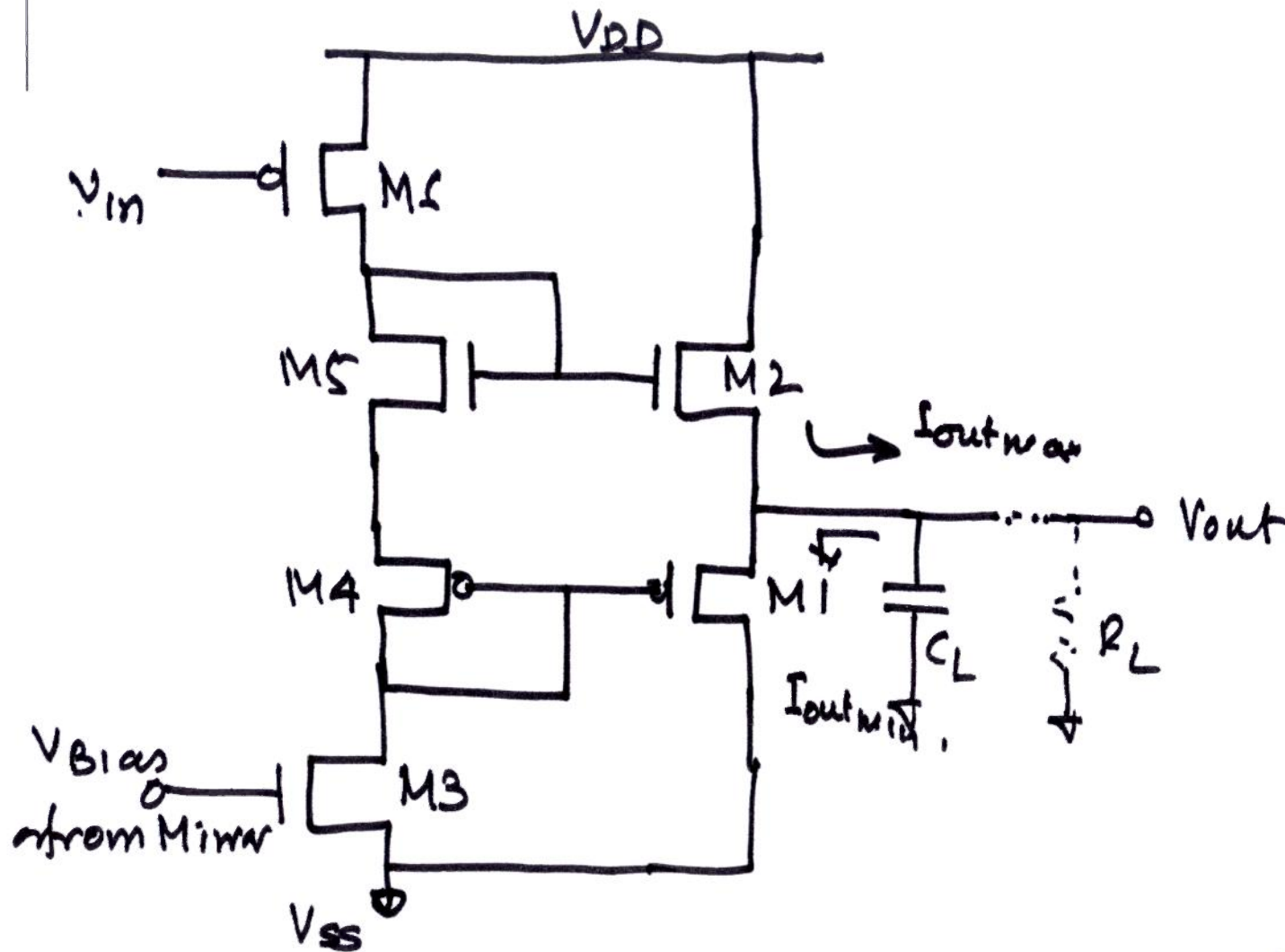
and 
$$V_{omin} = V_{SS} + V_{TP}$$

The implementation of  $V_{GA1}$  &  $V_{GA2}$  can be realised by a simple circuit embedded in this class AB (or B) Amplifier



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M1 & M2 Size  
decides  
 $I_{outmax}$  &  $I_{outmin}$ .

Class AB output Amplifier

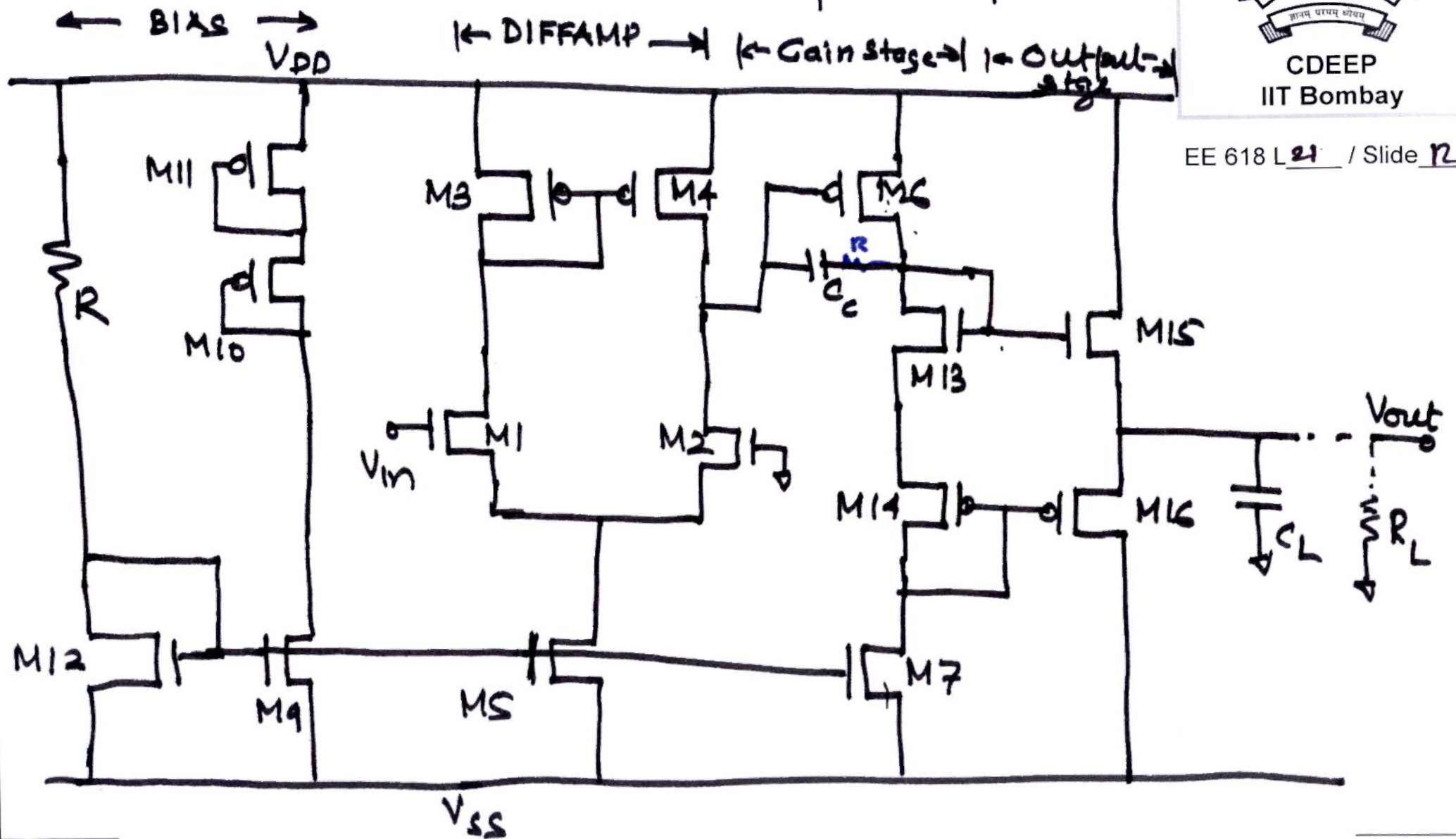
$$I_{outmax} = \frac{\beta_n}{2} (V_{ovn})^2 \quad \Delta \quad I_{outmin} = \frac{\beta_p}{2} (V_{ovp})^2$$

Basic CMOS OPAMP DESIGN can be extended to OPAMP with Output Amplifier



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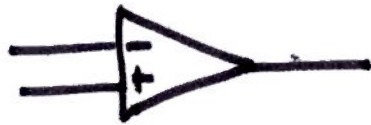
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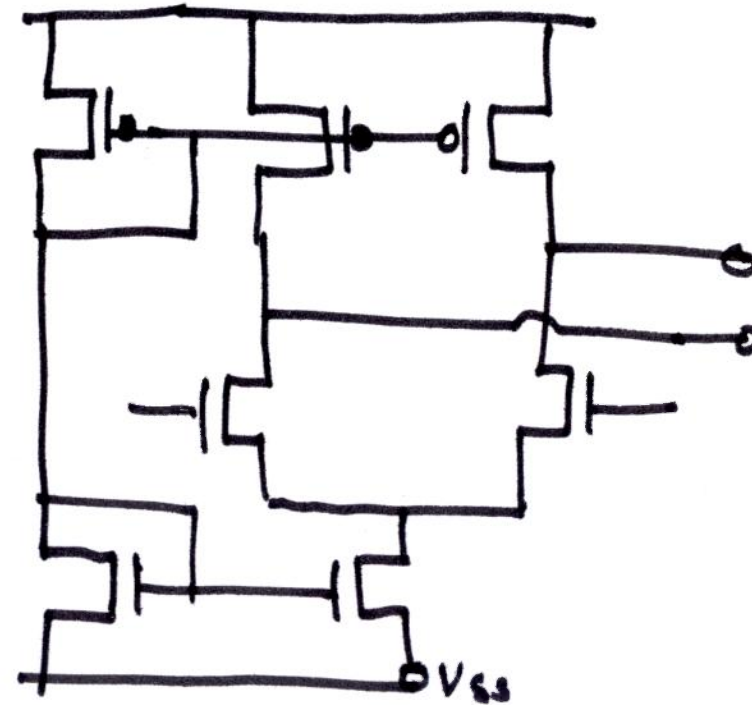
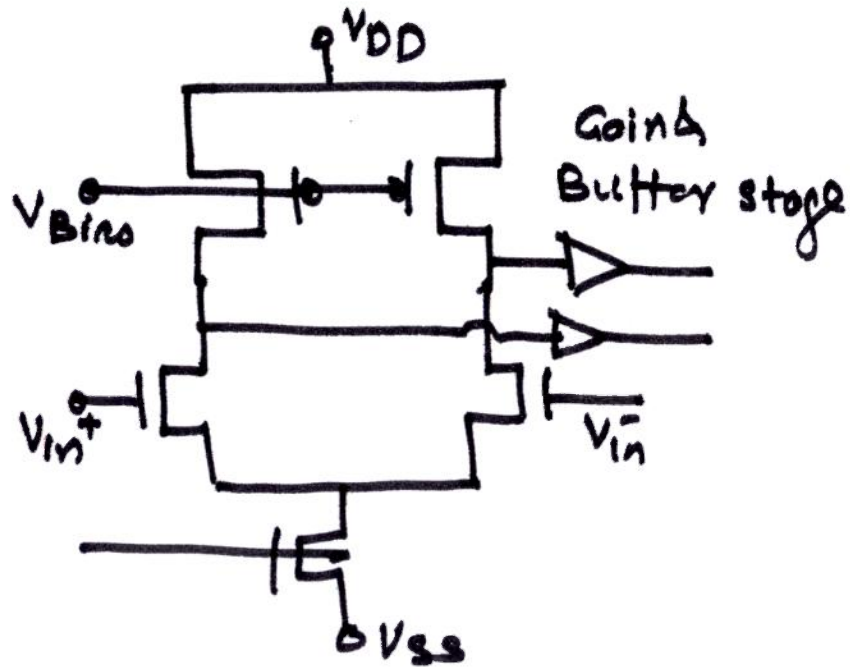
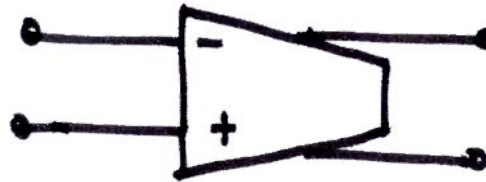
# OPERATIONAL Transconductance Amplifiers

## OTA

OPAMP



OTA



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## OPAMP

- 1 • OTA + Buffer
- 2 • VCVS ( $A_v$ )
- 3 • Low Output Resistance
- 4 • Drive possible for R & C loads
- 5 • Larger Power Dissipation & Complex Circuit
- 6 • Useful in most General Purpose Applications

## OTA

OTA

VCCS ( $G_m$ )

High Output Impedance

Drive Possible only Capacitive loads  
but not Resistive Loads

On chip Amplifiers  
are normally OTAs

Useful in realisation  
of Active  $g_m$ -C filters.



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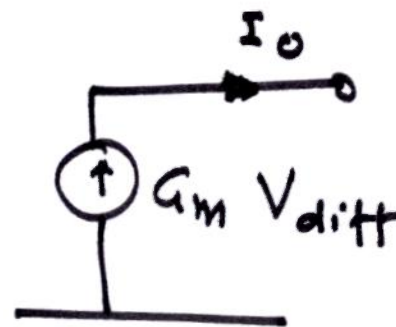
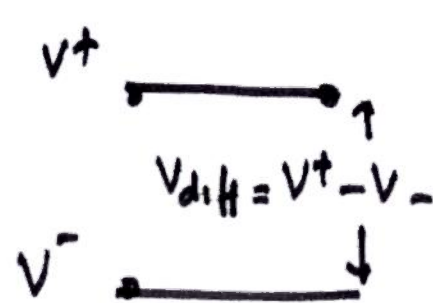
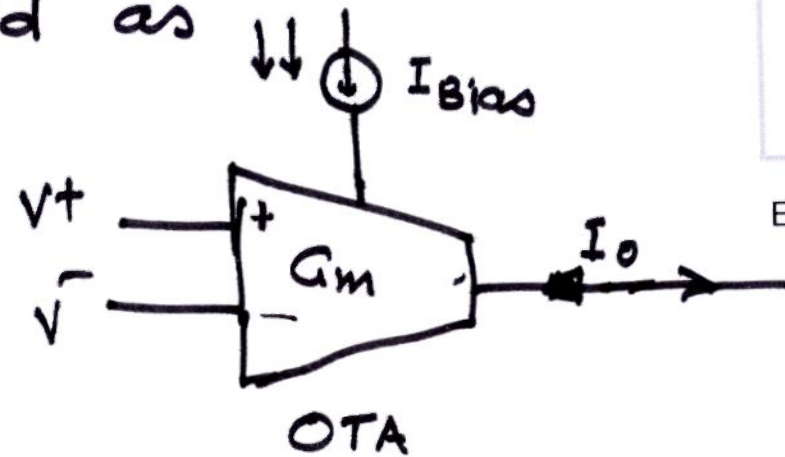
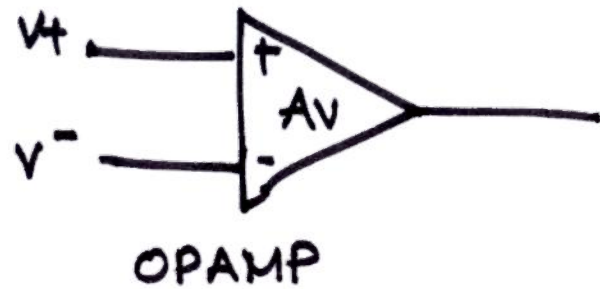
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As said earlier OTA is VCCS, and hence can be represented as



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$$\therefore I_o = G_m (V_+ - V_-) =$$

$$\therefore \boxed{\frac{I_o}{V_{diff}} = G_m}$$

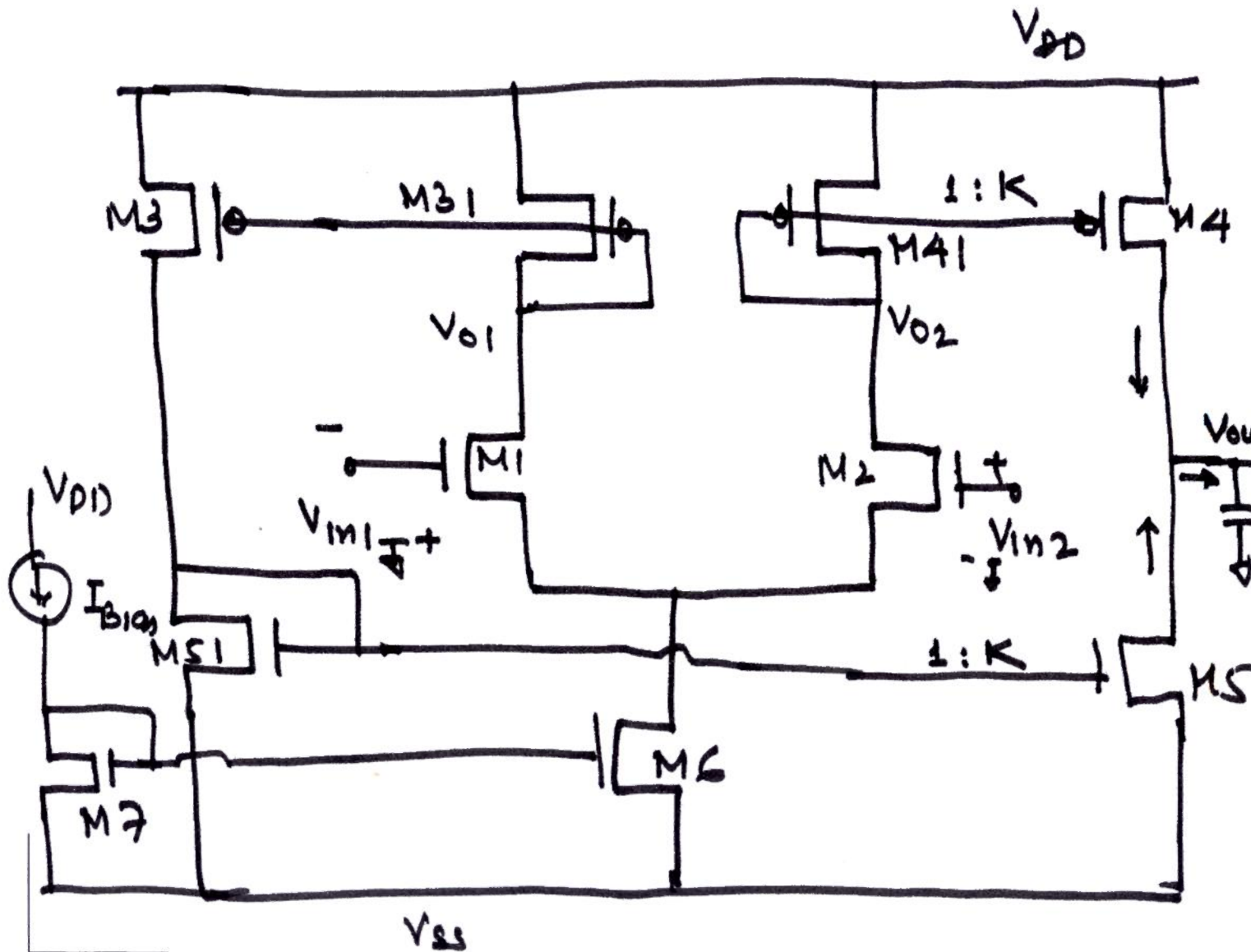
Transconductance Amplifier

# Typical Circuit of OTA



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We have initially

$$\beta_{n1} = \beta_{n2}$$

$$\beta_{p31} = \beta_{p41}$$





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By small signal Analysis, we observe that

$$i_{ds31} = -\frac{g_{m1}}{2} (V_{in2} - V_{in1}) \quad \text{--- (i)}$$

$$\text{But } i_{ds31} = -i_{ds41} = -\frac{g_{m1}}{2} (V_{in2} - V_{in1}) \quad \text{--- (ii)}$$

We also have the following relations

$$\beta_4 = \beta'_{p4} \left(\frac{W}{L}\right)_4 = K \beta'_p \left(\frac{W}{L}\right)_{41} \quad \text{--- (iii)}$$

$$\text{or } \beta_4 = K \beta_{41} = K \beta_{31} = K \beta_3 \quad \text{--- (iv)}$$

$$\beta_5 = K \beta_{51} \quad \text{--- (v)}$$

Clearly currents in M4 and M5 are out of phase

$$\therefore i_{ds4} = -i_{ds5} = K i_{ds41} = -K i_{ds31}$$

Output impedance at  $V_{out}$ ,

$$R_{out} = (r_{o4} \parallel r_{o5}) \parallel \left( \frac{1}{j\omega C_L} \right)$$

If  $\frac{1}{j\omega C_L}$  is quite high then

$$R_{out} \cong (r_{o4} \parallel r_{o5})$$

We define  $i_{ds} = -i_{ds31} = i_{ds41} = \frac{g_{m1}}{2} (V_{in2} - V_{in1})$

Then  $i_{out} = i_{ds4} - i_{ds5} = (K i_{ds41}) - (+K i_{ds31})$

$$i_{out} = 2K i_{ds} = 2K \cdot \frac{g_{m1}}{2} (V_{in2} - V_{in1})$$

or  $\frac{i_{out}}{V_{in2} - V_{in1}} = G_M = K \cdot g_{m1} \quad \left\{ \begin{array}{l} \text{Transconductance} \\ \text{- Gain} \end{array} \right\}$



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And then Voltage Gain  $A_{vo}$  is

$$A_{vo} = \frac{V_{out}}{V_{in2} - V_{in1}} = \frac{2K i_{ds} \cdot (r_{o4} \parallel r_{o5})}{V_{in2} - V_{in1}}$$
$$= \frac{2K \cdot \frac{g_{m1}}{2} (V_{in2} - V_{in1}) (r_{o4} \parallel r_{o5})}{(V_{in2} - V_{in1})}$$

$$A_{vo} = K g_{m1} (r_{o4} \parallel r_{o5})$$

If one chooses  $K = 1$  (Equivalent of OPAMP case)

Then  $G_M = g_{m1}$  &  $A_{vo} = g_{m1} (r_{o4} \parallel r_{o5})$

Since  $g_{m1} = \sqrt{2 \beta_1 I_{SS}} = \sqrt{2 \beta'_n \left(\frac{W}{L}\right)_1 \cdot \frac{I_{DS1}}{2}}$

We choose  $I_{DS1} = 2 I_{Bias}$



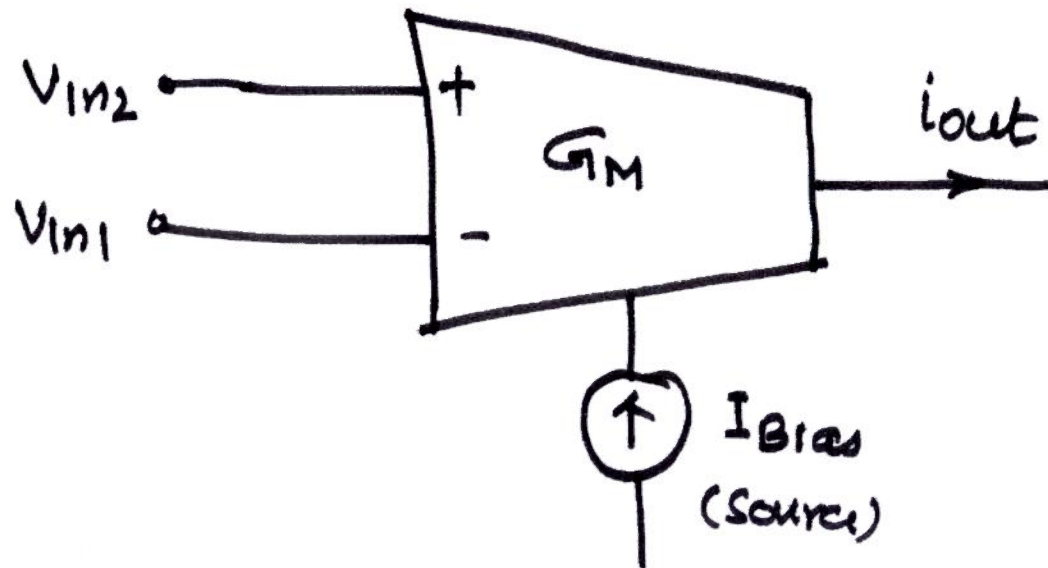
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Then  $g_{m1} = \sqrt{2\beta_1 \left(\frac{W}{L}\right)_1 I_{Bias}}$

or  $g_{m1} \propto \sqrt{I_{Bias}}$

or  $G_M \propto \sqrt{I_{Bias}}$



OTA Symbol.



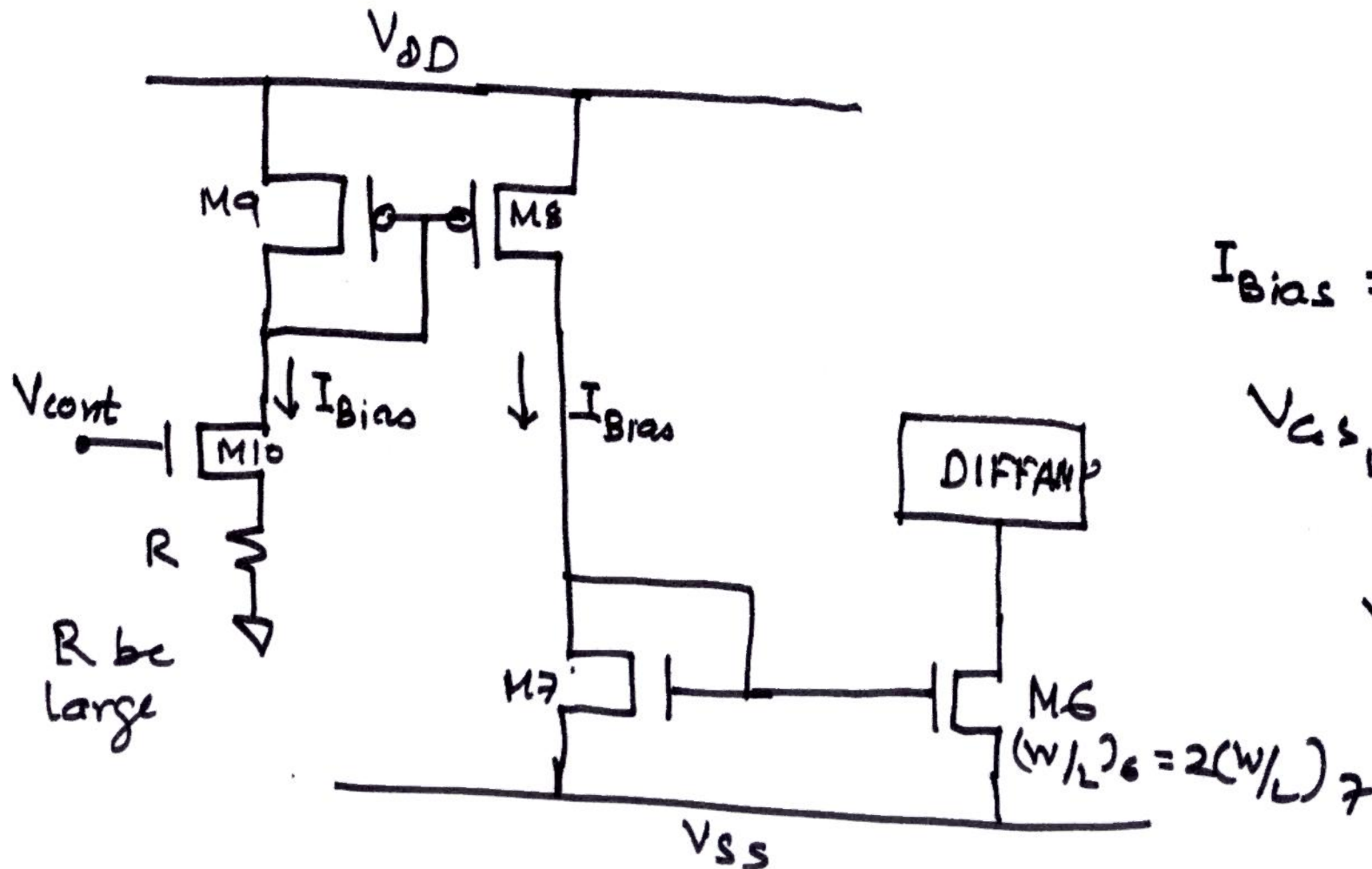
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Typically  $I_{Bias}$  is created using some control voltage  $V_{cont}$ , which can have circuit as



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$$I_{Bias} = \frac{V_{cont} - V_{as10}}{R}$$

$$V_{as10} \approx V_T$$

If  $(\frac{W}{L})_{10}$  is  
v. large (100-200)