Voltage References

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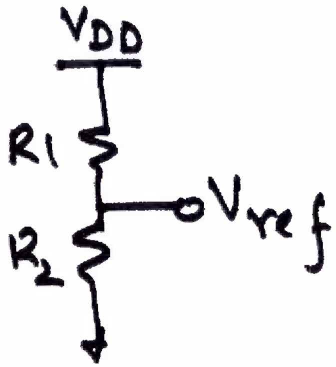
1. Divider Reference with Resistors



$$V_{ref} = \frac{R_2}{R_1+R_2} V_{DD} = \frac{1}{1+\frac{R_1}{R_2}} V_{DD}$$

$$\therefore \quad \frac{dV_{ref}}{dV_{DD}} = \frac{R_2}{R_1+R_2}$$

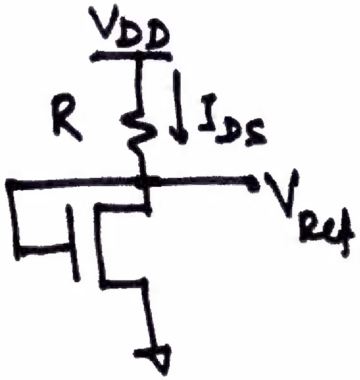
$$S_{V_{DD}}^{V_{ref}} = \frac{V_{DD}}{V_{Ref}} \cdot \frac{\partial V_{ref}}{\partial V_{DD}} = \frac{R_1+R_2}{R_2} \cdot \frac{R_2}{R_1+R_2} = 1$$

We see $\dfrac{\partial V_{ref}}{V_{ref}} = \dfrac{\partial V_{DD}}{V_{DD}}$ [% change in V_{DD} directly reflect in % variation of V_{ref}]

$$\therefore \quad TC_f(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{R_1}{R_2} \frac{V_{ref}}{V_{DD}} \left(\frac{1}{R_2}\frac{\partial R_2}{\partial T} - \frac{1}{R_1}\frac{\partial R_1}{\partial T} \right)$$

$$= \frac{R_1}{R_2} \frac{V_{ref}}{V_{DD}} \left[TC_f(R_2) - TC_f(R_1) \right]$$

Voltage Reference with MOSFET & Resistor



Clearly $V_{GS} = V_{Ref}$

& $I_{DS} = \dfrac{V_{DD} - V_{Ref}}{R}$

But $I_{DS} = \dfrac{\beta}{2}(V_{ov})^2$ for Transistor

$\therefore \quad V_{DD} - V_{ref} = \dfrac{\beta}{2} R \left[V_{ref} - \cancel{\tfrac{\beta}{2}R}\, V_T \right]^2$

Solving

$$V_{Ref} = V_T + \sqrt{\frac{2}{\beta R}(V_{DD} - V_{Ref})}$$

If $V_{DD} \gg V_{Ref}$

Then $V_{Ref} = V_T + \sqrt{\dfrac{2}{\beta R}}\, V_{DD}^{1/2}$

Then $$S^{V_{ref}}_{V_{DD}} = \frac{V_{DD}}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial V_{DD}}$$

$$\cong \frac{1}{V_T \cdot \sqrt{\frac{2\beta R}{V_{DD}}} + 2}$$

Further

$$TC_f(V_{ref}) = \frac{1}{V_{Ref}} \cdot \frac{\partial V_{Ref}}{\partial T}$$

$$= \frac{1}{V_{Ref}} \left\{ \left[V_T \, TC_f(V_T) - \frac{1}{2} \sqrt{\frac{2}{W/L} \frac{V_{DD}}{R\,\beta'(T)}} * \right. \right.$$

$$\left. * \left[\frac{1}{R} \frac{\partial R}{\partial T} - \frac{1.5}{T} \right] \right\}$$

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Then $I_Q R = V_{Tn} + \sqrt{\dfrac{2 I_Q}{\beta_n' (W/L)_1}}$

$$\therefore \quad (I_Q R - V_{Tn})^2 = \frac{2 I_Q}{\beta_n' (W/L)_1}$$

$$\text{or} \quad I_Q^2 R^2 + V_{Tn}^2 - 2 I_Q R V_{Tn} - \frac{2 I_Q}{\beta_n' (W/L)_1} = 0$$

One solution is

$$\therefore \quad I_Q = \frac{V_{Tn}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R}\sqrt{\frac{2 V_{Tn}}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}} = I_1 = I_2$$

and other solution is

$$I_Q = 0 \quad \text{giving} \quad I_1 = I_2$$

This is trivial solution, but can occure in reality.

Since M3 & M4 are chosen to be Identicle (Same β and V_T), with the mirror connected combination, $\therefore I_1 = I_2$, where I_1 flows from V_{DD} to V_{SS} (0V) through M5 and M1 and I_2 flows similarly from M4 – M2 and through R.

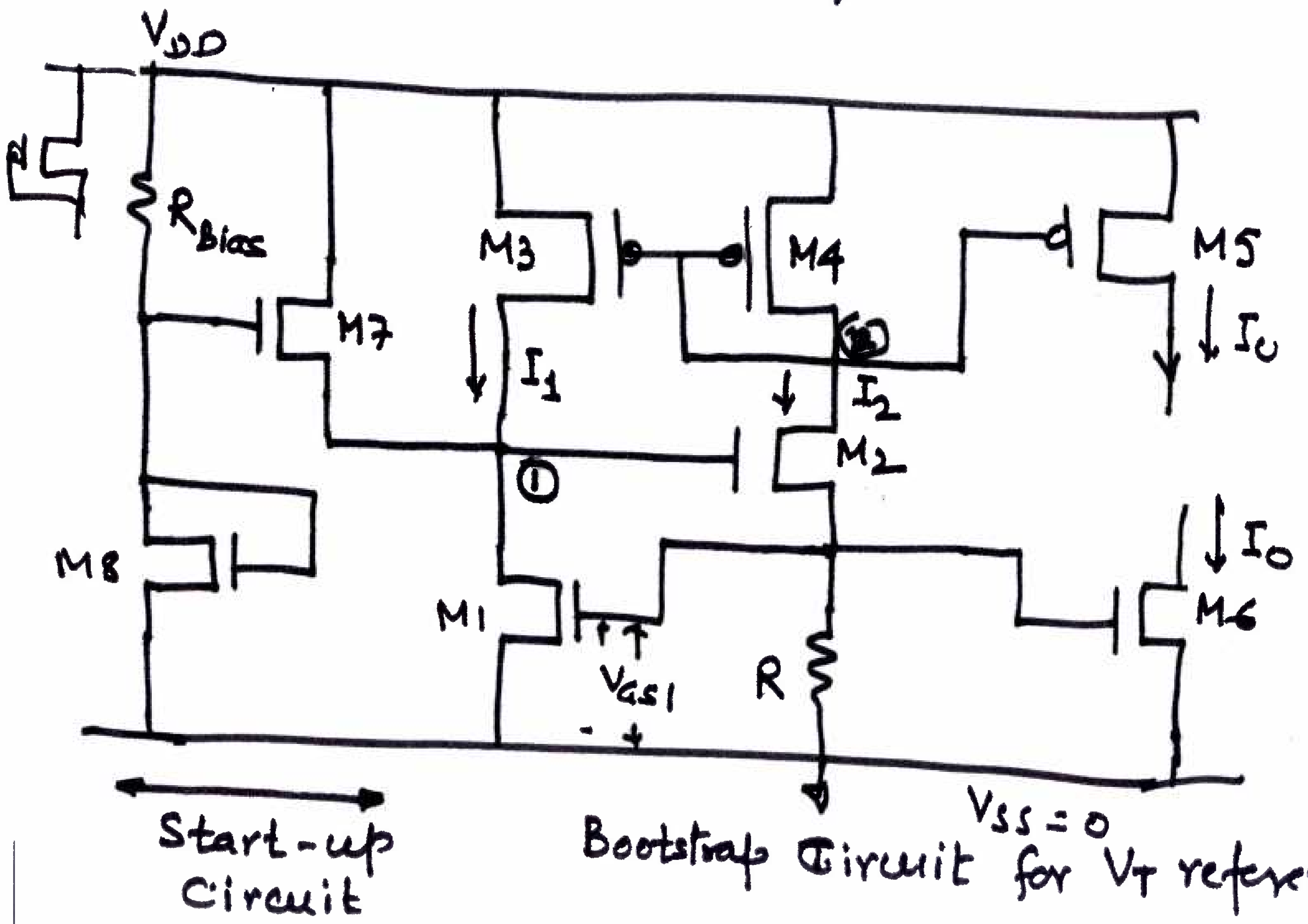
Clearly $V_{GS1} = I_2 \cdot R$ or $= I_1 R$

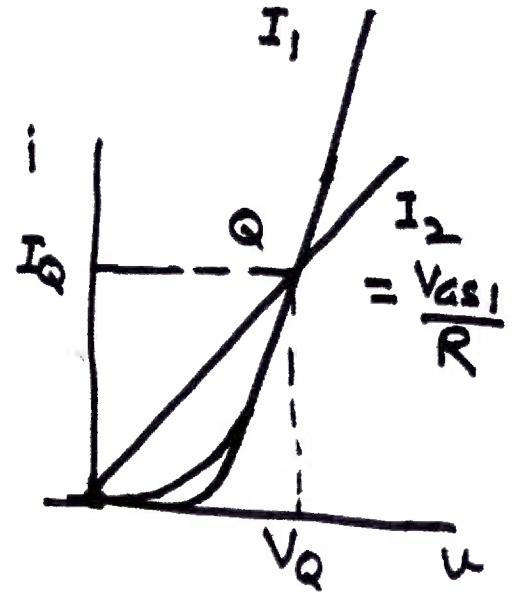
But $V_{GS1} = V_{Tn} + \sqrt{\dfrac{2 I_1}{\beta_n'(W/L)_1}}$

$$\therefore \quad I_2 R = I_1 R = V_{Tn} + \sqrt{\frac{2 I_1}{\beta_n'(W/L)_1}}$$

We define $I_1 = I_2 = I_Q$

A Better V_T reference is possible using Bootstrap Technique.





Bootstrap Circuit for V_T reference.

In case of $I_1 = I_2 = I_Q = 0$, we see that we need a Start-up circuit.

Transistor M7 is 'ON' when initially Node (1) is at '0' V. Thus M7 provides current to M1. This increases V_{GS1} of M1, which in turn increases I_2 $\left(\frac{V_{GS1}}{R}\right)$. By feedback (& Mirror) action Node (1) voltage starts increasing ($V_{GS1}+V_{GS2}$) and at one time V_{GS} for M7 goes below V_{T7}, thereby shutting off M7. Here the Q point of Reference reaches second stable point. Further Starting Circuit then stops participating.

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If R is created from Polysilicon Layer (n^+),

then $TC_f(R) = \frac{1}{R}\frac{dR}{dT} \cong -2000\ ppm/^\circ C$

The β-Multiplier circuit thus show

$$TC_f(I_o) = -2 \times 2000 + \frac{1.5}{T\,(^\circ K)}$$

$$= +1000\ ppm/^\circ C \quad \text{at } T = 300^\circ K$$

We can use this circuit as Voltage Reference V_{REF} equal to V_{GS1}

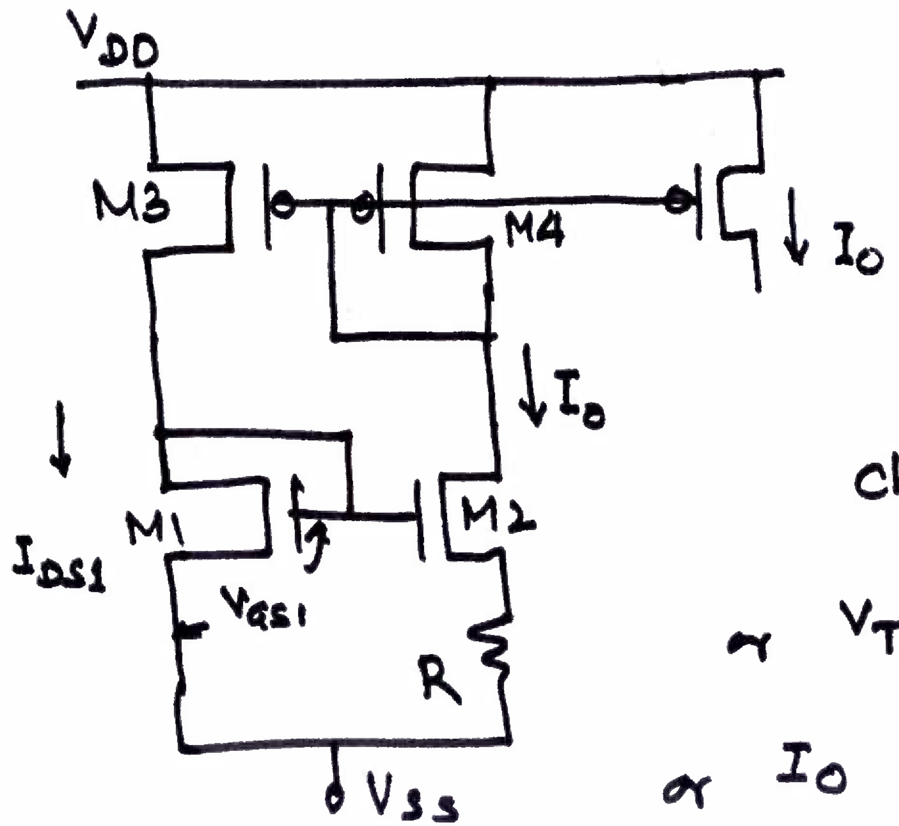
$$V_{REF} = V_{GS1} = \frac{2}{\beta_1 R}\left(1 - \frac{1}{\sqrt{K}}\right) + V_{Tn}$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{Tn}}{\partial T} + \frac{2}{\beta_1 R}\left(1 - \frac{1}{\sqrt{K}}\right)\left[\frac{1}{R}\frac{dR}{dT} + \frac{1}{\beta_1}\frac{\partial \beta_1}{\partial T}\right]$$

β - Multiplier V_{REF}.

This scheme is also called Self - Biasing Scheme

This also uses 'Starting Circuit' for Operation to begina.



$I_{DS1} = I_o$

Here Width of M2, W_2 is chosen K times of Width W_1 of M1

or $\beta_2 = K\,\beta_1$

Clearly $V_{GS1} = V_{GS2} + I_o R$

or $V_{Tn} + \sqrt{\dfrac{2 I_o}{\beta_1}} = V_{Tn} + \sqrt{\dfrac{2 I_o}{K \beta_1}} + I_o R$

or $I_o = \dfrac{2}{R^2 \beta_1}\left(1 - \dfrac{1}{\sqrt{K}}\right)^2$

We can find value of K, for $\frac{dV_{REF}}{dT} = 0$

Thus choice of K can give $TC_f(V_{REF}) = 0$

Corresponding

$$V_{REF} = V_{Tn} + \frac{2}{R\beta_1}\left[1 - \frac{1}{\sqrt{K}}\right]$$

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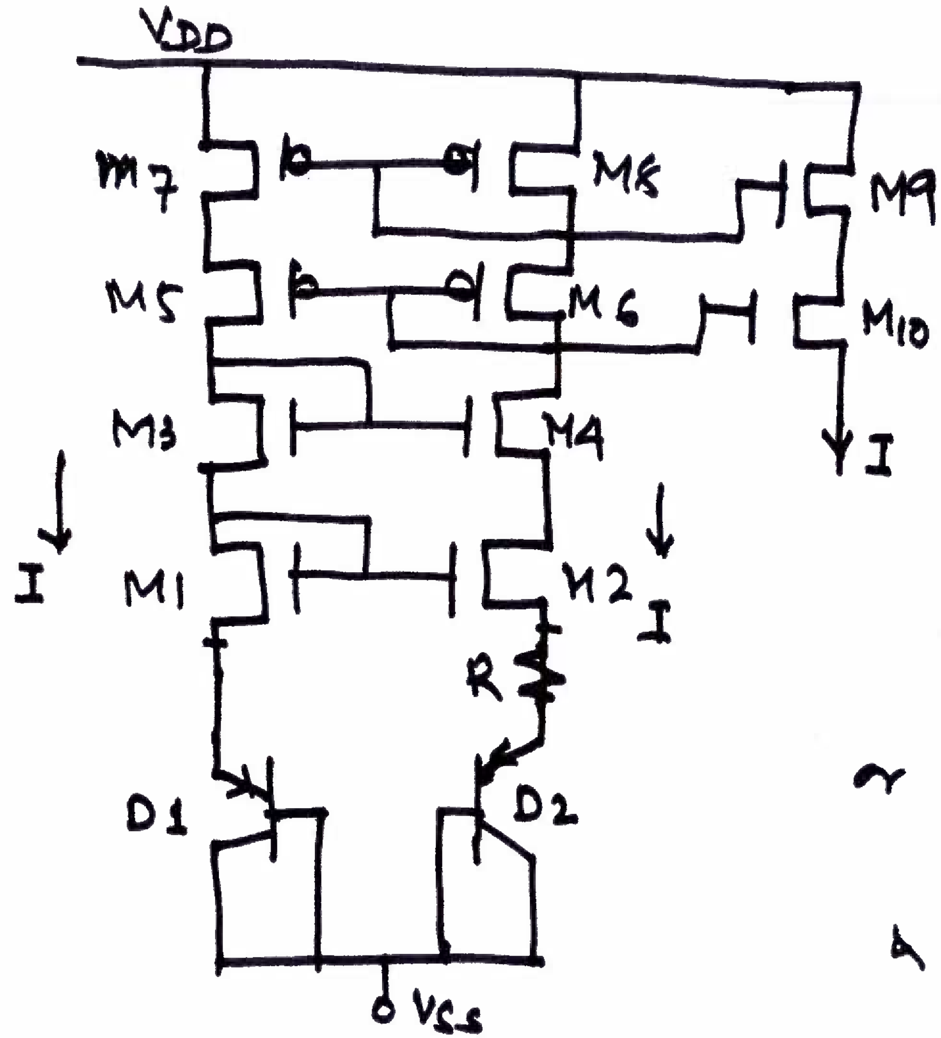
PTAT Current Biasing Scheme



As $V_{GS1} = V_{GS2}$ for same current in M1 & M2

Also $\beta_2 = K\beta_1$ $(W_2 = K W_1)$

$\therefore V_{GS1} = V_{DS1} = IR + V_{DS2}$ — (1)

Diode currents are

$$I_{D1} = I = I_{sat}\, e^{qV_{BE}/kT\cdot n}; \quad V_{BE} = V_{DS1}$$

or $V_{DS1} = \dfrac{nkT}{q} \ln \dfrac{I}{I_{sat}}$

& $V_{DS2} = \dfrac{nkT}{q} \ln \dfrac{I}{K \cdot I_{sat}}$ (2)

Substituting (2) in (1)

$$\frac{\eta kT}{q} \ln \frac{I}{I_{sat}} = \frac{\eta kT}{q} \ln \frac{I}{K \cdot I_{sat}} + IR$$

$$\frac{\eta kT}{q} \ln \frac{(I/I_{sat})}{(I/K I_{sat})} = IR$$

or $$IR = \frac{\eta kT}{q} \ln K$$

or $$I = \frac{\eta kT}{qR} \cdot \ln K$$

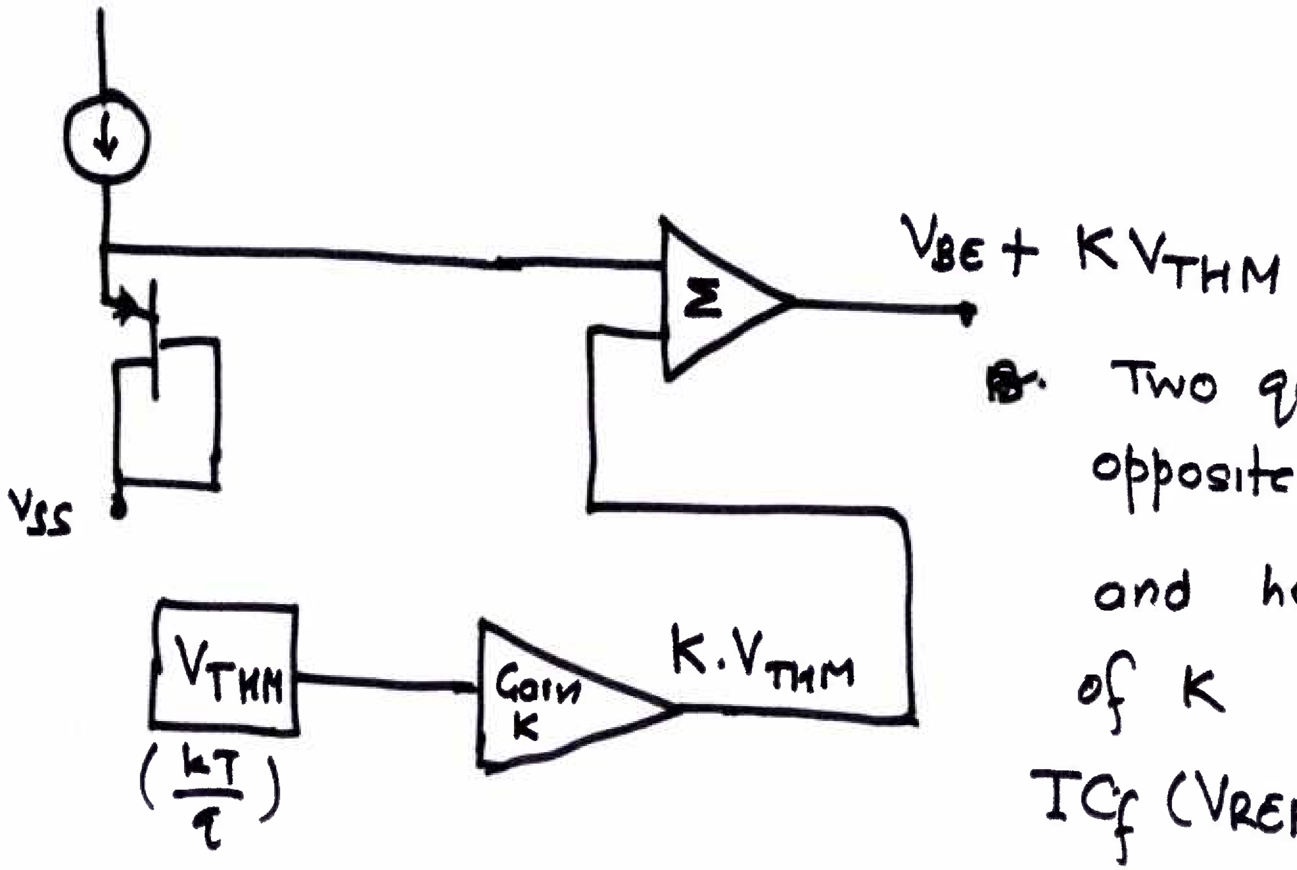
$$= \frac{V_{Thermal}}{R} \cdot \ln K$$

$\eta = 1$ for Silicon diode in Active Mode (Diffusion current only)

$\therefore\ I \propto T$ (Proportional To Absolute Temperature)

$TC_f(I) \sim 1000\ ppm/^\circ C$

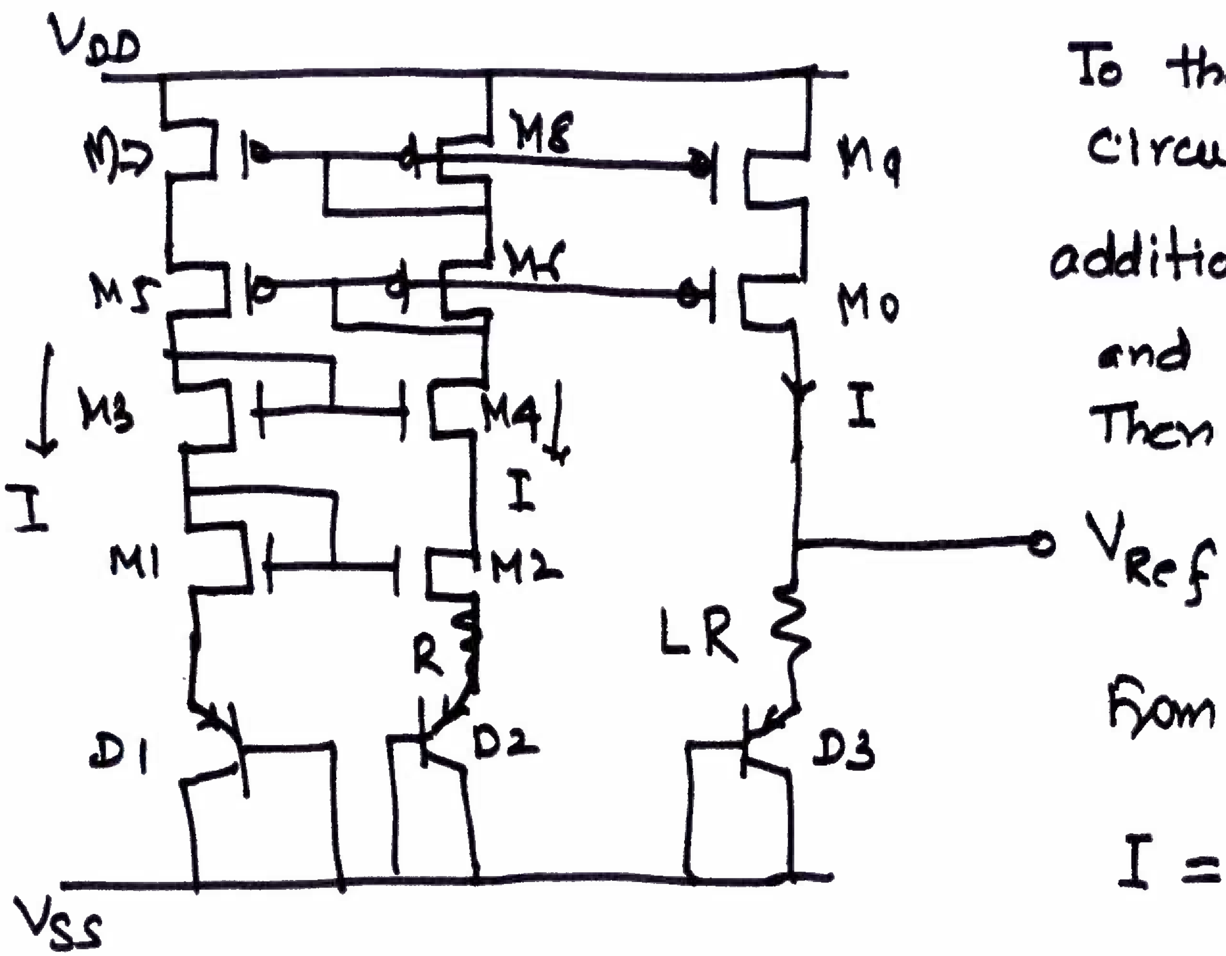
Principle of BANDGAP REFERENCE



- Two quantities have opposite Polarity TC_f and hence by adjustment of K

$TC_f(V_{REF}) \rightarrow 0$

Bandgap Reference Circuit



$$V_{Thermal} = \frac{kT}{q}$$

To the PTAT circuit, we have additional resistance LR and Diode D3 in output arm. Then we get V_{Ref} with near $TC_f(V_{Ref}) \rightarrow 0$

From PTAT ckt

$$I = \frac{V_{Thermal}\ \ln(K)}{R}$$

Then $V_{Ref} = V_{D3} + I \cdot L \cdot R$

$$= V_{D3} + \frac{L\, V_{Thermal}}{1} \ln K$$

$$V_{D3} = \frac{nkT}{q} \ln \frac{I}{K I_{sat}}$$

$$\therefore V_{REF} = L \cdot V_{THM} \cdot \ln K + V_{THM} \ln \frac{I}{K I_{sat}}$$

$$= V_{THM} \left[L \ln(K) + \ln \frac{I}{K I_{sat}} \right]$$

For normal diode in CMOS Technology, with $L = 12$ & $K = 8$

we get $V_{REF} = 1.25V$ (Bandgap of Silicon)

Further $\frac{dV_{REF}}{dT} = {}^{+}$ value $-$ value. If Adjust K, L is done $\rightarrow = 0$