# Module – 5

# UNIT -5

# Field Effect Transistors

## Review Questions:

1. Draw the structure of JFET and discuss its working.
2. What is ‘pinch off’ voltage? How to get its value experimentally?
3. An n-JFET is operated with negative gate voltage and not with positive one. Give reasons.
4. Give the structure of depletion MOSFET (D - MOSFET). How is D - MOSFET different from enhancement MOSFET (E - MOSFET)?
5. Draw and discuss drain characteristics for a D-MOSFET.
6. Discuss the formation of channel in E-MOSFET emphasizing the role of inversion layer.
7. Give self bias circuit for JFET and explain the biasing process.
8. How can we obtain negative or positive bias voltage with proper choice of resistors in a voltage divider bias?
9. Develop a simple small signal model/equivalent circuit for FET.
10. How are DMOSFET and EMOSFET connected in a circuit to work as resistors?
11. Derive expression for voltage gain for a common source amplifier.
12. Illustrate power efficiencies of CMOS devices through a CMOS inverter circuit.

## Problems:-

**5.1** The device parameters for an n-Channel JFET are: Maximum current $I_{DSS}$ = 10mA, Pinch off voltage,

$V_p$ = - 4V

Calculate the drain current for

(a) $V_{GS}$ = 0

(b) $V_{GS}$ = - 1.0v

(c) $V_{GS}$ = - 4V.

## Solution:-

The expression for drain current $I_D$, in the saturation region is,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad ..................(A)$$

(a) When $V_{GS}$ = 0, from Eq(A) above,

$$I_D = I_{DSS} = 10mA$$

(b) When $V_{GS}$ = -1.0V, the drain current from Eq (A) is,

$$I_D = 10\times 10^{-3}\left[1-\left(\frac{-1}{-4}\right)\right]^2$$
$$= 10mA \times 0.56$$
$$or\ I_D = 5.6\ mA$$

(c) When $V_{GS}$ = -4V = $V_p$, then from Eq(A),

$$I_D = I_{DSS}\left[1-\left(\frac{-4}{-4}\right)\right]^2$$
$$or,\ I_D = 0$$

**5.2** A JFET produces gate current of 2nA when gate is reverse biased with 8V. Determine The resistance between gate and source.

## Solution:-

Since reverse gate-source voltage, $V_{GS}$, of 8v produces gate current, $I_G$ of 2nA, Therefore, gate-to-source resistance, $R_{GS}$, is

$$R_{GS} = \frac{V_{GS}}{I_G} = \frac{8V}{2nA} = 4000M\Omega$$

$$R_{GS} = 4000M\Omega$$

**5.3** The reverse gate voltage of JFET when changes from 4.4V to 4.2V, the drain current changes from 2.2 mA to 2.6 mA. Find out the value of transconductance of the transistor.

## Solution:-

The transconductance, $g_m$ is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Where $\Delta I_D$ is change in drain current when change in gate-source voltage is $\Delta V_{GS}$.

In the given problem,

$\Delta I_D$ = (2.6 – 2.2) mA

= 0.4 mA

And,

$\Delta V_{GS}$ = (4.4 – 4.2) V

= 0.2 V

Therefore,

$$g_m = \frac{0.4\,mA}{0.2V}$$

$$or\ ,\ g_m = 2.0\,m\ \ mhos.$$

**5.4** Find out the operating point current and voltage values ($I_{DQ}$ and $V_{DSQ}$) for a self biased JFET having the supply voltage $V_{DD}$ = 20V and maximum value of drain current as 12 mA.

## Solution:-

We know that the value of drain current at Q-point may be taken as half of the maximum current, that is,

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{12mA}{2} = 6.0\,mA$$

In the same way, the value of drain-source voltage at Q-point may be taken as half of supply voltage $V_{DD}$. That is,

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{20V}{2}$$

$$or,\ V_{DSQ} = 10V$$

Therefore,

$I_{DQ}$ = 6.0 mA

$V_{DSQ}$ = 10.0 V

**5.5** Calculate the value of source resistance $R_S$ required to self bias a n-JFET such that $V_{GSQ}$ = - 3V. The n-JFET has maximum drain-source current $I_{DSS}$ = 12 mA, and pinch-off voltage, $V_p$ = - 6V

## Solution:-

The drain current, $I_D$, in a JFET, in the saturation region is,

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$$

We have, $I_{DSS}$ = 12 mA, $V_{GS}$ = -3V and $V_p$ = -6V, Therefore,

$$I_D = 12mA\left[1-\left(\frac{-3}{-6}\right)\right]^2$$

$$or,\ I_D = 9.0\ mA$$

Since the voltage $V_{GS}$ is generated across the source resistor $R_S$, we have,

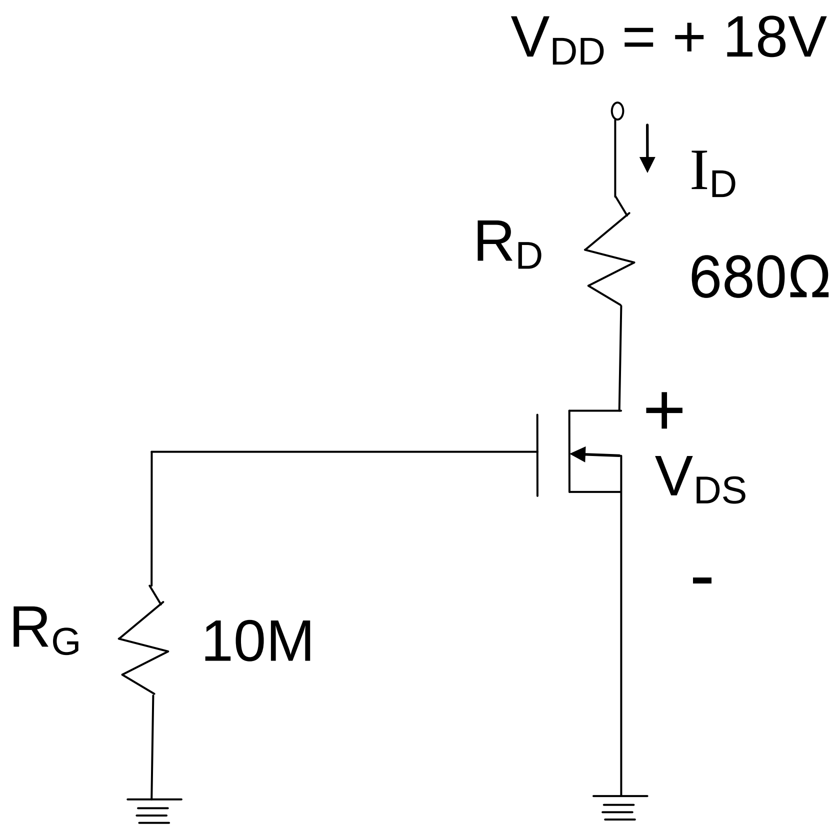
$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{3V}{9\,mA} \simeq 333\Omega$$

$$R_S \simeq 333\Omega$$

**5.6** For the DMOSFET circuit shown in fig., the device parameters are:

$V_{GS(off)}$ = -8V, $I_{DSS}$ = 10mA

Determine drain-to- source voltage $V_{DS}$.



## Solution:-

In a MOSFET, there is no gate current. Therefore, there is no voltage drop across resistor $R_G$ .

Thus, $V_{GS} = 0$.

Further, when $V_{GS} = 0$, $I_D = I_{DSS}$, the maximum drain current.

Summing up voltages in the output loop and using $I_D = I_{DSS}$,

We have,

$I_{DSS} . R_D + V_{DS} = V_{DD}$

or $V_{DS} = V_{DD} - I_{DSS} . R_D$

$= 18 - 10 \times 10^{-3} \times 0.68 \times 10^{3}$

$= 18 - 6.8$

or $V_{DS} = 11.2$ V

**5.7** Data sheet of an EMOSFET specifies following parameters:

$I_{D(on)}$ = 50 mA at $V_{GS}$ = 6V and $V_T$, the threshold voltage for EMOSFET, 2V.

Determine the drain current at $V_{GS}$ = 3V.

## Solution:-

We first determine the conductance parameter k for the device using the relation,

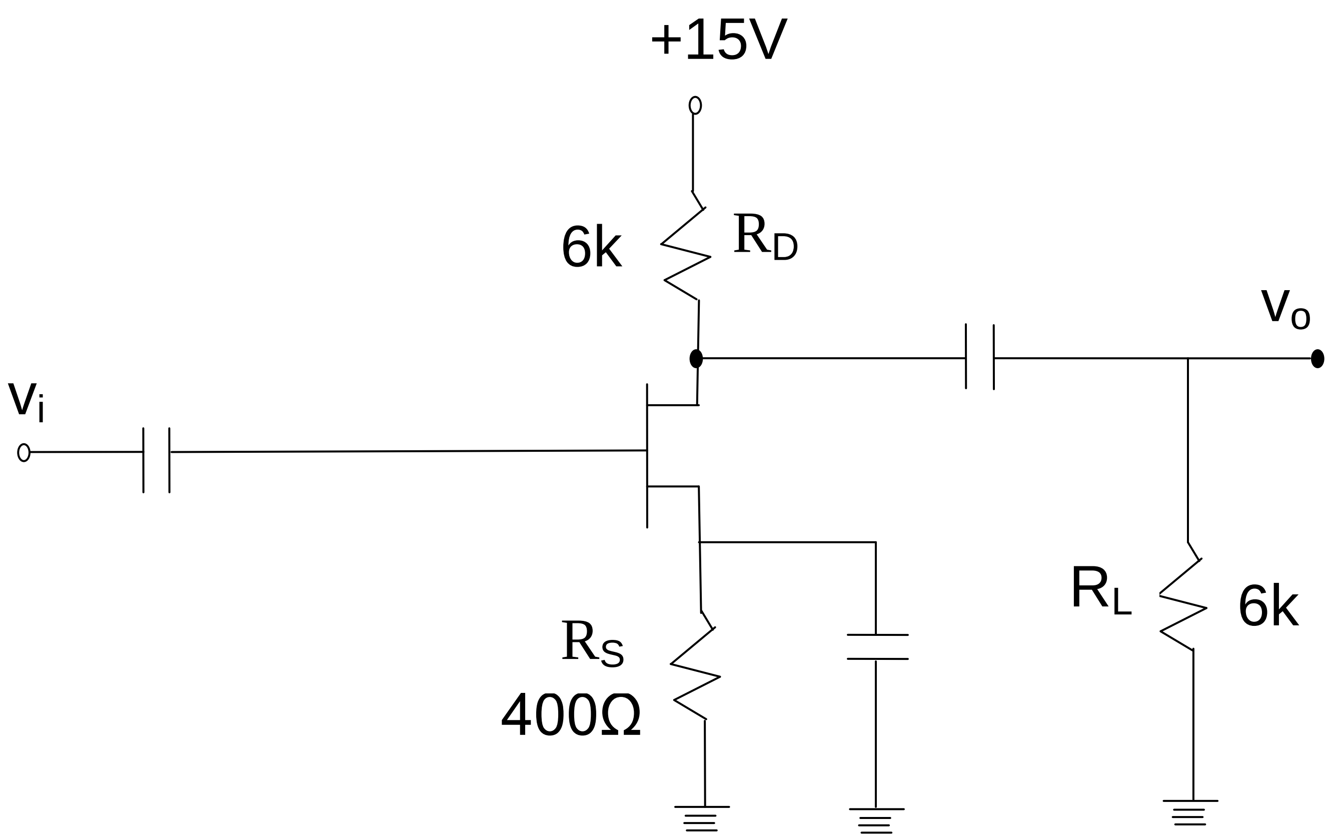
$$
\begin{aligned}
k &= \frac{I_{D(ON)}}{\left(V_{GS} - V_T\right)^2} \\
&= \frac{50\,mA}{(6-2)^2} \\
or,\ k &= 3.12\ {mA}/{v^2}
\end{aligned}
$$

Now, the drain current, $I_D$ is expressed as,

$$
\begin{aligned}
I_D &= k\left(V_{GS} - V_T\right)^2 \\
&= 3.12\times10^{-3}\,(3-2)^2 \\
or,\ I_D &= 3.12\ mA
\end{aligned}
$$

**5.8** The drain current changes from 5 mA to 7 mA when the gate voltage is changed from – 4.0V to – 3.7V in the amplifier circuit shown in fig.

Calculate the voltage gain of the amplifier.



## Solution:-

In case, the source resistance $R_S$ is ac grounded as done in the circuit of fig. the gain of amplifier is,

$A_V = g_m . r_D$

Where $g_m$ is transconductance of the transistor and $r_D$ is effective ac resistance seen by the drain terminal.

Now,

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$$

$$= \frac{2\,mA}{0.3V}$$

$$or,\ g_m = 6.66\,mS$$

And,

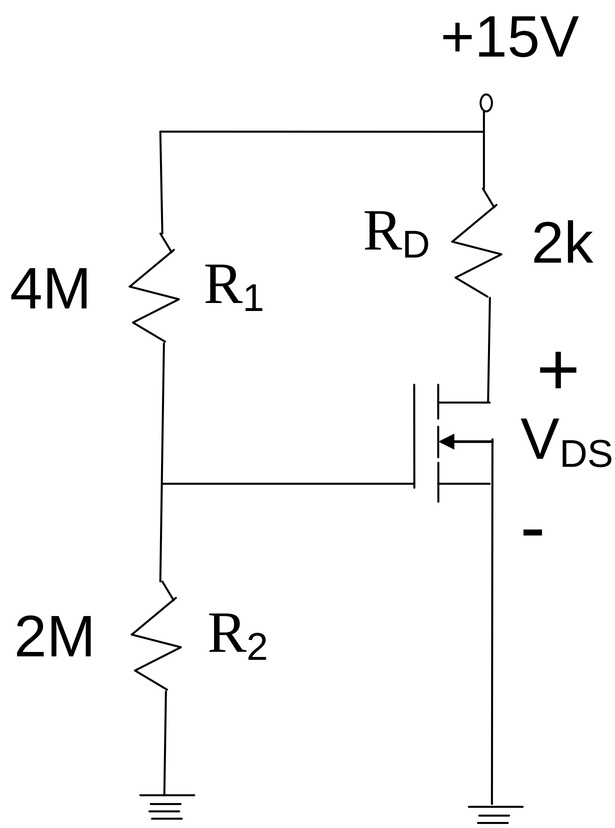
$r_D = R_D || R_L = 6k || 6k = 3k\Omega$

Therefore,

$A_V = g_m \times r_D = 6.66 \times 10^{-3} \times 3 \times 10^{3}$

or, $A_V = 20$

**5.9** Find the drain-source voltage, $V_{DS}$, for the NMOS transistor circuit shown in fig. The device parameters are: conductance parameter, k = 600μA/v$^2$ and $V_T$ = 2V.



## Solution:-

The gate current, $I_G$, is zero in a MOSFET. Then, from voltage divider network,

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$$
$$= \left(\frac{2M\Omega}{4M\Omega + 2M\Omega}\right) \times 15V$$
$$or, V_{GS} = 5V$$

And, as we know

$$I_D = k\ V_{GS} - V_T\ ^2$$
$$= 600 \times 10^{-6} \times (5-2)^2$$
$$= 5.4\ mA$$
$$or,\ I_D = 5.4\ mA$$

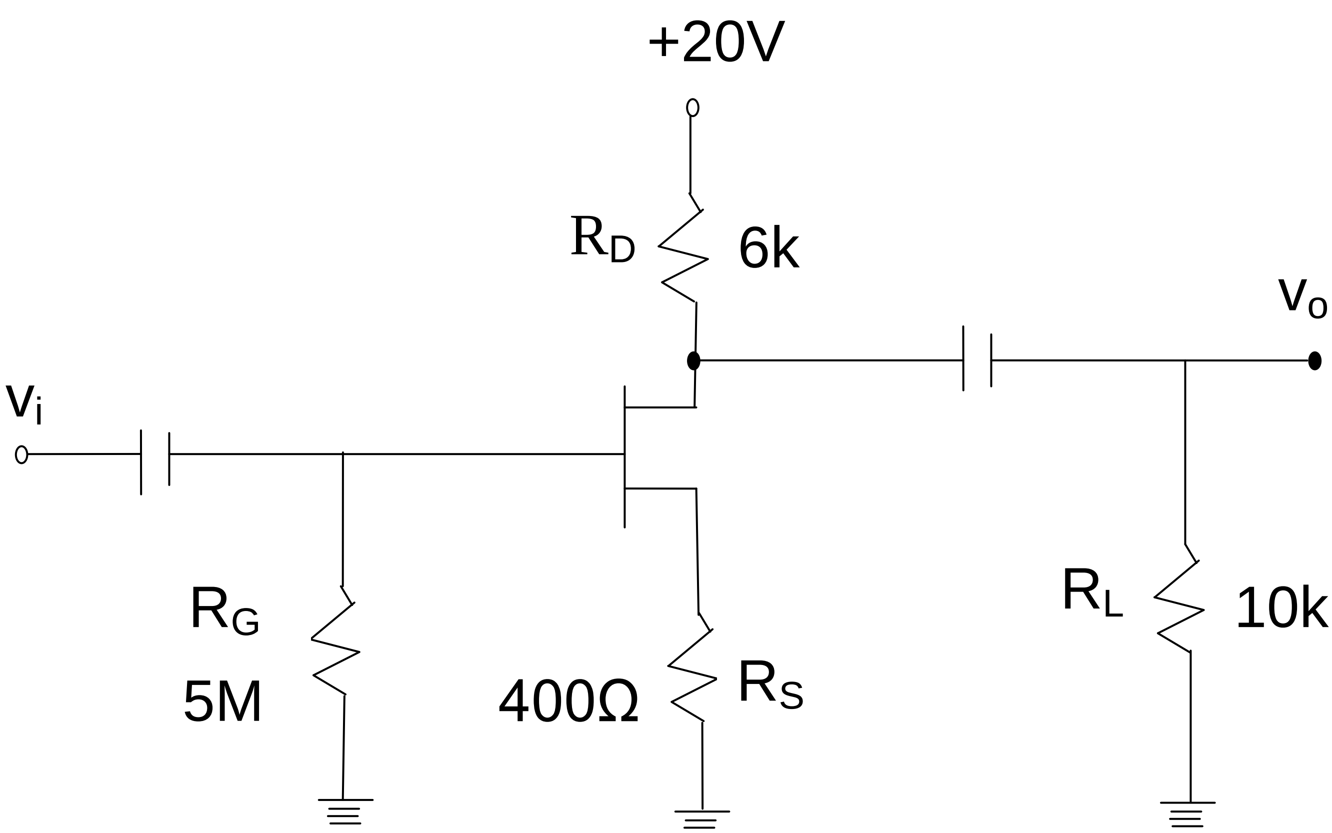
Applying voltage summation in the output loop,

$V_{DD} = I_D R_D + V_{DS}$

or, $V_{DS} = V_{DD} – I_D R_D = 15 – (5.4 \text{ X } 10^{-3} \text{ X } 2 \text{ X } 10^3)$

or, $V_{DS}$ = 4.2V

**5.10** Calculate the voltage gain in the amplifier shown in fig. The transconductance of the transistor is 4000μs. If the 400Ω source resistance is by passed by an capacitor, how much is voltage gain now?



## Solution:-

When the source resistance $R_S$ is not by passed, the voltage gain is,

$$A_V = \frac{g_m r_D}{1 + g_m r_s} \qquad ...........(A)$$

Where $r_D$ and $r_S$ are effective (ac) resistance seen by the drain and source of the transistor.

And,

$r_D = R_D \| R_L$

$= 6k \| 10\ k = 3.75\ k\Omega$

And,

$r_S = R_S = 400\Omega$

Therefore

$$A_V = \frac{4000 \times 10^{-6} \times 3.75 \times 10^{3}}{1 + 4000 \times 10^{-6} \times 400}$$

$$= \frac{4 \times 3.75}{2.6} = 5.7$$

$$A_V = 5.7$$

In case, $R_S$ is bypassed, the gain ($r_S = 0$ in the Eq(A)),

$A_V = g_m r_D = 4000 \text{ X } 10^{-6} \text{ X } 3.75 \text{ X } 10^{3}$

or, $A_V = 15$