Lecture-47

INTEL 8085A INTERRUPT STRUCTURE

There are five interrupt inputs TRAP, RST7.5, RST6.5, RST5.5 and INTR. TRAP is a non-maskable interrupt, that is, it cannot be disabled by an instruction. RST7.5, RST6.5, RST5.5 and INTR are maskable interrupts i.e. they can be enabled or disabled through software. The 8085A interrupt structure is shown in fig.8.8.

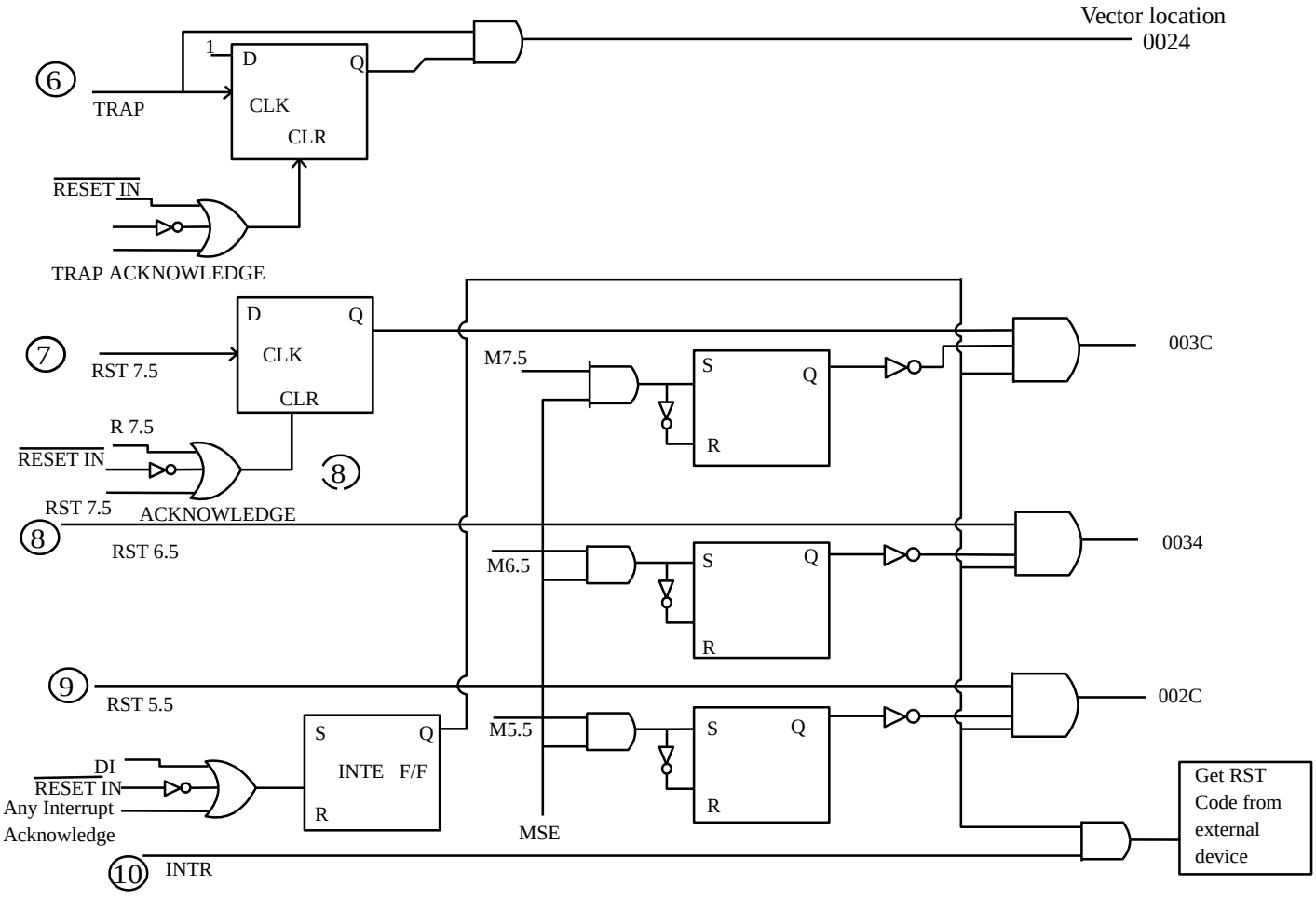

Fig.8.8 Interrupt Structure of Intel 8085A

The following flip-flops are internally provided in the interrupt system of the μp.

1. **R7.5 F/F:** The RST7.5 signal is a LOW to HIGH transition active interrupt control signal input. The LOW to HIGH transition of the signal is registered in R7.5 flip-flop. Thus R7.5 F/F provides a seat for RST7.5 interrupt. It is normally RESET when the power is on. Only LOW to HIGH transition of RST7.5 sets this R7.5 flip-flop to store interrupt. When M7.5 is RESET only then R7.5 signal can interrupt the processor. R7.5 flip-flop can be reset or cleared through the SIM instruction. It is for the user to make use of these facilities.

2. **MSE F/F:** A common chain MASK SET ENABLE (MSE) F/F is provided for all the interrupt masks. This flip-flop must be SET Mask set enable (MSE) flip-flop is also set. This flip-flop can be SET to '1' using SIM instruction for individually enabling or disabling the MASK doors.

3. **INTE F/F:** It is an interrupt enable flip-flop. When the power is turned ON for the first time, $\overline{\text{RESET IN}}$ signal goes LOW. It resets the processor 8085A. It also resets the INTE flip-flop so that the entire interrupt structure is disabled. The INTE F/F can be SET or RESET using instructions. When INTE F/F is RESET, except for TRAP no other interrupt signal can interrupt the processor. When the INTE F/F is SET, the interrupt system is enabled and other interrupt control signals can be selectively enabled or disabled.

4. **INTA F/F**: This is an Interrupt acknowledge flip-flop used only for internal operation by the microprocessor. When first the power is ON this F/F is reset by the $\overline{\text{RESET IN}}$ control signal. Thereafter, whenever a valid interrupt is recognized by the μp it always resets the INTE F/F and then sets the INTA F/F before further action. Thus, further interrupts shall not be recognized, unless, user through instructions in the programme desires further recognition of the interrupt.

5. **MASK F/F (M5.5, M6.5, M7.5):** M7.5, M6.5 and M5.5 are mask flip-flops. These Mask F/Fs are used individually to MASK the interrupts RST5.5, RST6.5 and RST7.5 When these F/Fs are individually SET, then the corresponding interrupt is masked and the interrupt control signal in question can not interrupt the μp. These mask flip-flops are SET to '1' during power ON by $\overline{\text{RESET IN}}$ control signal going LOW. These mask flip-flops can be individually and selectively clear to '0' through SIM instruction (SET INTERRUPT MASK) provided MSE F/F is also SET. MASK SET ENABLE F/F can be SET simultaneously using SIM instruction.

TRAP:

TRAP is a non-maskable vectored interrupt. It can interrupt the μp once the power is ON. Most μp interrupt inputs are level sensitive however, some are edge sensitive and others are both edge and level sensitive. The TRAP input is both edge sensitive and level

sensitive interrupt. It means that TRAP make a low to high transition and remain high until it is acknowledged. The positive edge of the TRAP signal sets the D flip-flop. Because of the AND gate, however the final TRAP also depends on a sustained high level TRAP input. This is why the TRAP is both edge and level sensitive. This also avoids false triggering caused by noise and transients.

For example, suppose the 8085A is midway through an instruction cycle with another 2μsec to completion. If a 300nsec noise spike hits the TRAP input, it will edge triggered but not level trigger the TRAP interrupt because 8085A is still working on the current instruction cycle. Because the TRAP is both edge and level sensitive the 8085A avoids responding to false TRAPs.

Since the TRAP input has the highest priority, it is used for catastrophic events such as power failure, parity errors, and other events that require immediate attention. In the case of brief power failure it may be possible to save critical data. With parity errors, the data may be re-sampled or corrected before going on.

Whenever TRAP comes, μp completes the current instruction, pushes the program counter on the top of the slack and branches to fixed location 0024H. Once the 8085A microprocessor recognizes a TRAP interrupt, it will send a high TRAP ACKNOWLEDGE bit to the TRAP F/F, thus clears the F/F so that even if TRAP remains high it is not recognized again and again. It is further recognized only if it goes low, then high and remains high. The TRAP F/F is also cleared when μp is being reset during which $\overline{\text{RESET IN}}$ goes low and clears the F/F.

RST7.5, RST6.5 & RST5.5:

These are maskable vectored interrupts. These interrupts can be enabled or disabled through software. RST 7.5 has the highest priority among these & RST5.5 has the lowest priority.

RST7.5 control signal input is a rising edge sensitive interrupt. Whenever LOW to HIGH transition occurs, it can interrupt the microprocessor. This LOW to HIGH transition is registered in second D flip-flop. The output of this flip-flop is labeled I7.5. Whenever the other inputs are high the μp recognizes this interrupt. This request is remembered until

1. the processor 8085A responds to the interrupt. When interrupt is acknowledged, it sends a high RST7.5ACKNOWLEDGE bit to the clear input of D flip-flop. This clears it for future interrupts.
2. or until the request is RESET by SIM instruction. R7.5 bit is made high through SIM instruction and the flip-flop can be cleared. It is for the user to make use of these facilities.
3. or until the μp is being reset i.e., $\overline{\text{RESET IN}}$ signal becomes low. Whenever RST7.5 is recognized, control is transferred to 003CH.

RST6.5 & RST5.5 are also vectored and maskable interrupts but are HIGH level sensitive interrupt control signal inputs. These are directly connected to AND gate. The signal at these inputs must be maintained until the interrupt is acknowledged. Whenever RST6.5 is recognized, the control is transferred to 0034H & whenever RST5.5 is recognized, the control is transferred to 002CH.

The internal control signals I7.5, I6.5 & I5.5 are called pending interrupts. The signal IE (output of bottom flip-flop) is called interrupt enable flag. It must be high to activate the AND gates. Also, notice the M7.5, M6.5 & M5.5 signals. They must be low to enable the AND gates. e.g., to activate RST7.5 interrupt, I7.5 must be high, M7.5 must be low and IE must be high.

The interrupt enable flip-flop can be set or reset through software. This flip-flop can be set using EI instruction. EI stands for enable interrupt. Whenever EI is executed, it produces a high EI bit and sets the INTE F/F and produces a high IE output. This flip-flop can be reset in three ways.

1. When the power is ON for the first time or $\overline{\text{RESET IN}}$ signal goes low, it resets the INTE F/F so that that entire interrupt structure is disabled. When INTE F/F is reset except for TRAP no other interrupt can interrupt the μp.
2. The INTE F/F can be reset using DI instruction. DI stands for disable interrupt. When executed it produces a high DI bit & clear the INTE F/F.
3. When the processor 8085A recognizes an interrupt, it produces a high ANY INTERRUPT ACKNOWLEDGE bit. This disables the interrupts.

Because the interrupts are automatically disabled by the ANY INTERRUPT ACKNOWLEDGE bit, programmer usually includes an EI as the next to last instruction in the service subroutine so that the interrupt structure is enabled again. For instance, the last two instructions of interrupt service subroutines typically are

Subroutine: :

:

EI

RET

This subroutine cannot be interrupted (except by a TRAP). After the EI is executed, the processing returns to the main program with the interrupt system enabled.

INTR:

INTR is a maskable interrupt. A high on this pin interrupts the processor. The interrupt signal input INTR is not affected by SIM instruction. Only INTE F/F must be SET to '1' before this interrupt comes.

With the above explanation can write the logic expression for the logic variable, VALID INT

VALID INT = 0 when none of the interrupt control signal input are interrupting the.

VALID INT = 1 when any of the interrupt control signal is active.

Thus, in 8085A, we can write the logical expression for the LOGIC variable VALID INT as below:

VALID INT = TRAP + INTE.[INTR + R75. $\overline{M7.5}$ + RST6.5. $\overline{M6.5}$ + RST5.5. $\overline{M5.5}$]