Semiconductor Manufacturing
ISSUES

Semiconductor Manufacturing is constrained by Requirement of Very Very Clean enviroment during processes. The place where such 'clean' or rather 'Super Clean' enviroment is created is called "CLEAN-ROOM".

All IC manufacturing Companies have Three Step approach to control of Contaminants.

1. CLEAN-ROOM [OF Desired "Class"]
2. Wafer Cleaning
3. Gettering

contaminants may be classified as

1. Particles 2 Surface contaminants

3 Molecular contaminants

1 Particle contamination

(a) Major source are the people working in IC Labs.

(a_i) Skin prespiration (a_{ii}) Hair (a_{iii}) Clothing Lints

(b) Bare wood, cardboard products; Including Paper could be Source of Particles

(c) Any machine which produces 'sawing' or Sanding or Drilling.

2. Surface Contaminants

(a) finger's tips :- Oil and Grease

(b) Oil on body, Hairs

(c) Face-Cream, Wax

(d) Polish

(e) Face powder

3. Molecular Contaminants

(a) Out Gassing (b) Oil vapours (c) Paints, Glues & Epoxies

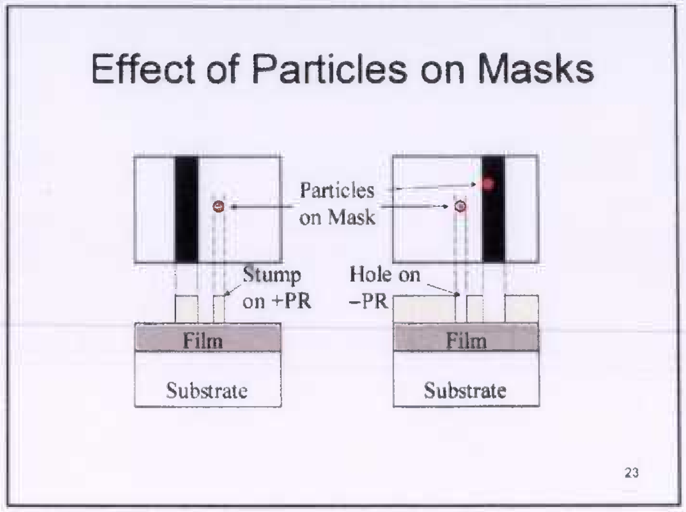
(d) Aromatics (e) Alcohol

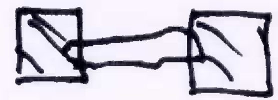
4. Inorganic & Organic Contamination due to equipments and Reagents in Lab.

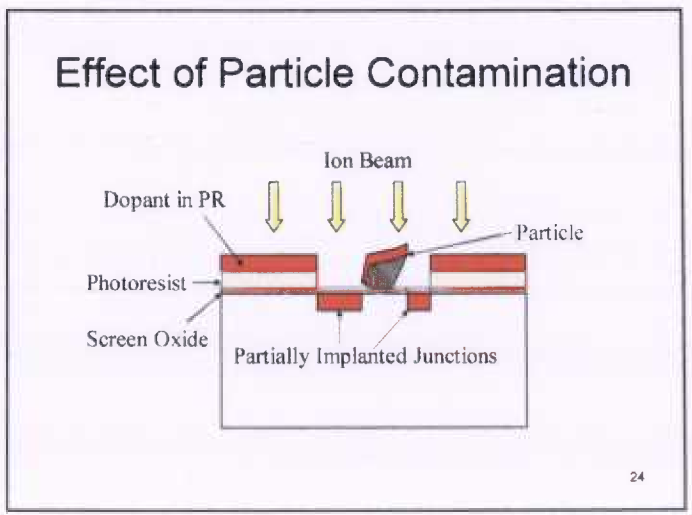
(a) Heavy Metals – Stainless Steel Pipes, Furnace front ends, other metallic impurities from Reagents

(b) from Water, Human prespiration and air, One gets Alkali Ions who occupy Silicon Surface. Na^+ and K^+ are likely alkali ions in the lab.

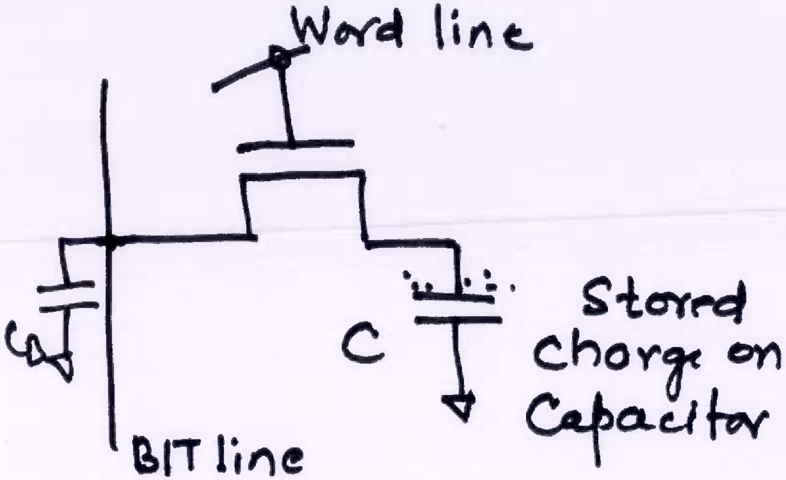
[A] Effect of Contaminants







[B] DRAM performance under contaminant environment



DRAM performance

:— Refresh time

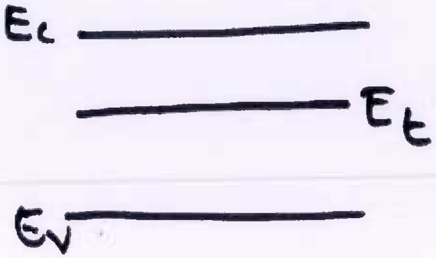
Access time

During Refresh cycle, the generation of electrons are needed in the MOS capacitor

For larger time elapse between Refresh Cycles, we need Generation time τ_G be High.

Further loss of DRAM charge is essentially due to Leakage currents. Leakage occures due to Recombination

The SRH mechanism is dominated due to Presence of Traps in Silicon. We know



$$\tau_R = \tau_G = \frac{1}{\sigma\, v_{th} \cdot N_t}$$

where N_t is Trap Density

for $\tau_R = \tau_G \geq 100\ \mu s \sim 1$ (or even higher) msec

Min $\tau_R = \tau_G$ as per SIA standards should be $\geq 25\ \mu sec$

For $v_{th} = 10^7$ cm/sec in Silicon, with Capture Cross section σ of the order of 10^{-15}, the Trap density N_t be $\simeq 10^{12}$/cc. (0.02 ppb). Typical traps availability are due to Na^+, K^+, Au and Fe as well as Cu. First two Na^+ & K^+ are mobile ions on the Surface

[C] Alkali ions (Mobile Ions) can get incorporated in Gate-Oxide & MOS structure. This may give variable V_T

$$V_{T_{n,p}} = \pm\phi_{ms} \pm 2\phi_F - \frac{Q_B + Q_{ox} + Q_m + Q_{it}}{C_{ox}}$$

$+$ m | Na^+ | Si $-$

Q_M is Mobile Ion (like Na^+) density in col./cm^2

Clearly if Q_M varies due to mobile ion movement, then V_T also varies proporationately.

PBTI and NBTI are known worries in MOS Flash ROMs.

Clean Room Concept

1. Site Infrastructure, facilities & Building
2. Power Supply needs and distribution
3. Electrical and Communication systems
4. Main Clean-Room area
5. Surrounding room areas
6. Central facilities
7. Process Utilities
8. Environment and Safety.

Space Allocation in Clean area

1. Lithography : 25 %
2. Diffusion & LPCVD : 20 %
3. Ion Implantation : 10 %
4. Thin film Deposition : 20 %
5. Dry Etching : 15 %
6. Wet-Cleaning areas : 10 %

http://www.nano.iisc.ernet.in/Semiconductor%20clean%20room_%20intro.pdf

Control of Contaminants by Clean-Air Control

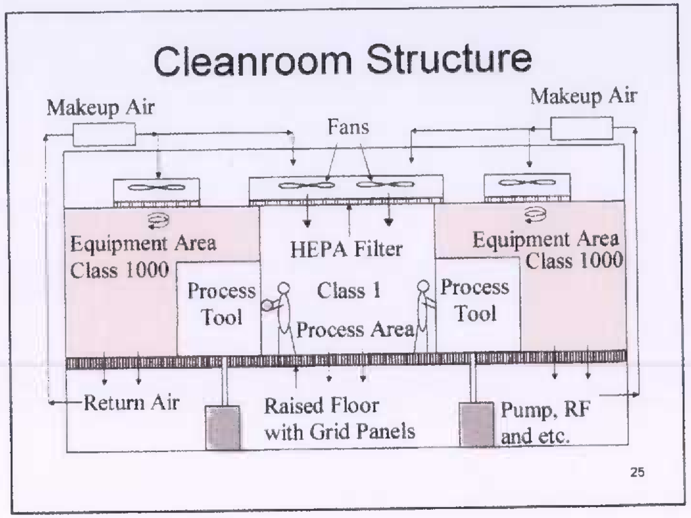
1 Air filter:
Class decides

2 . Air Conditioning
Temp. & Humidity
22°C & 40% RH

3 Air Pressure
> 30 Pascals
(> 0.25 torr)

4 Accoustic Noise
< 60 db

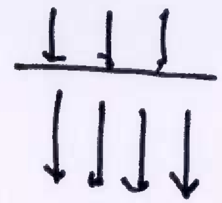
5 Vibrations
< 3 μm/sec



Mini-environment

- Class 1000 cleanroom, lower cost
- Boardroom arrangement, no walls between process and equipment
- Better than class 1 environment around wafers and the process tools
- Automatic wafer transfer between process tools

26



6. ESD < ± 50V

7. Magnetic field (mG) < ±1

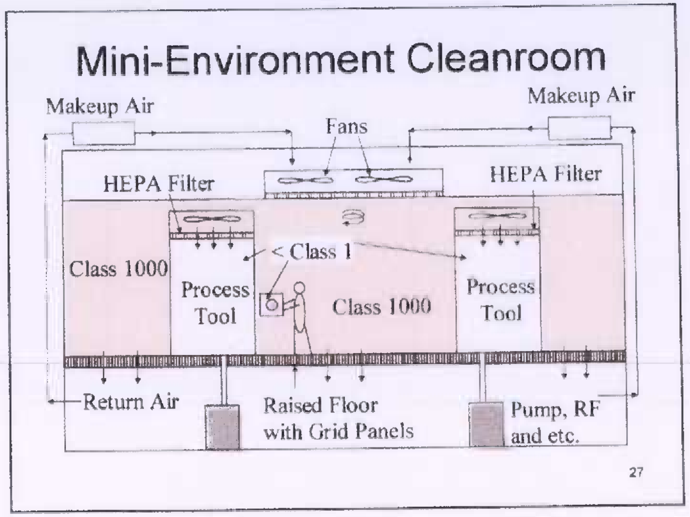
8 Hydrocarbons < 100 ppb

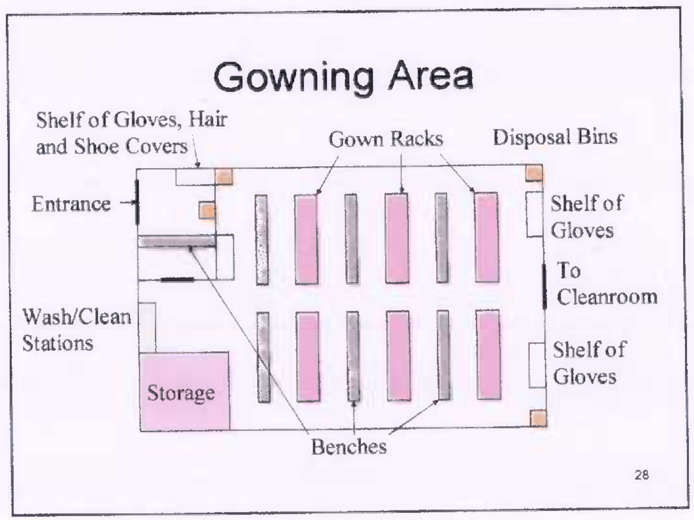
9 Other < 0.5 ppb

HEPA Filter →

High Efficiency Particulate Air Filter

Particle sizes 0.01 μ, 0.05 μ -- 5μ

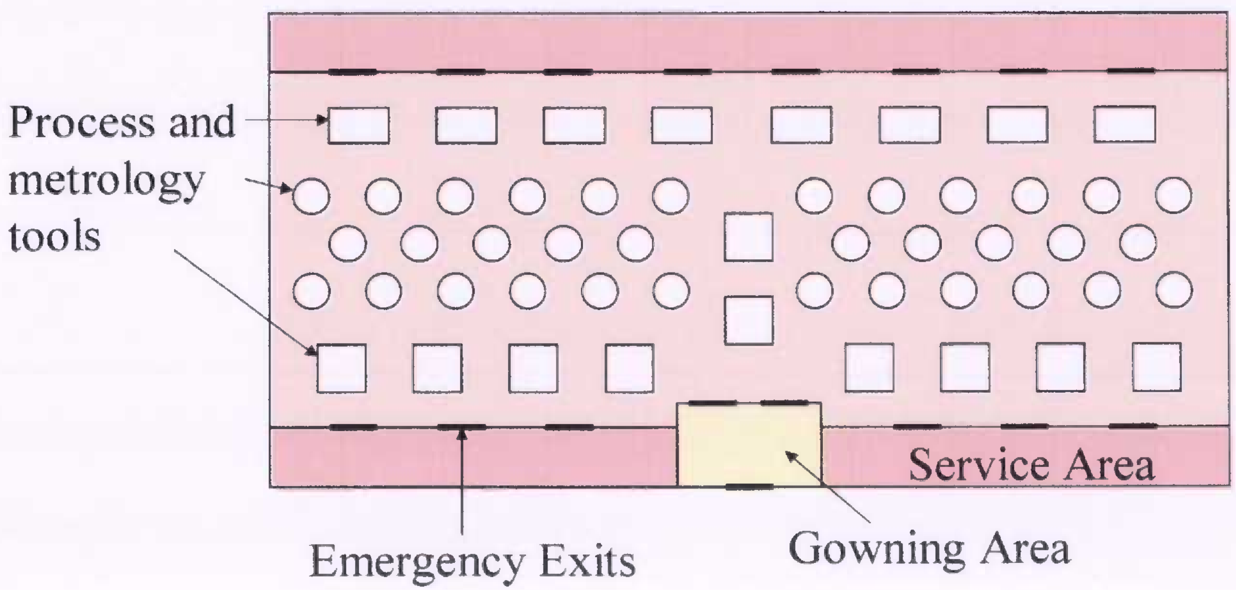




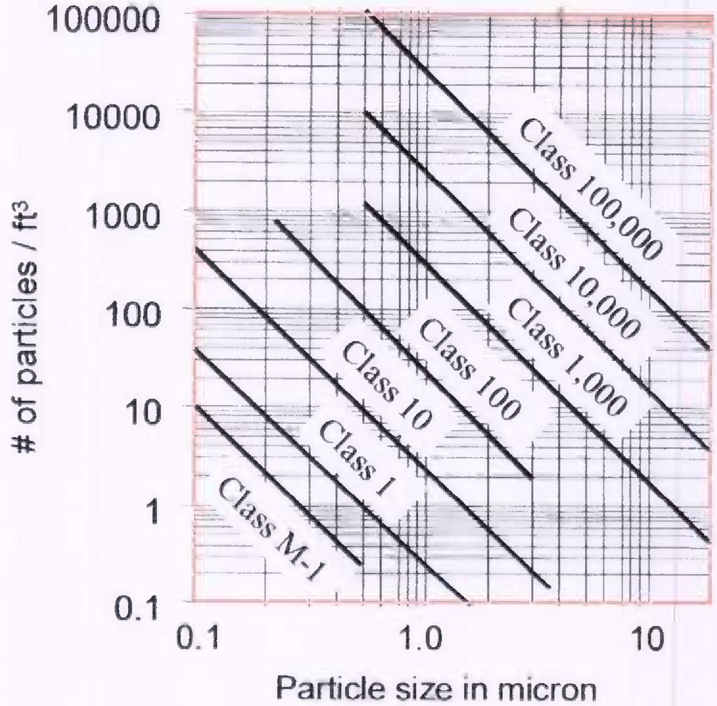
(a) 0.05 Hepa means 99.999999 % of 0.08 μm particles removed

(b) 0.01 HEPA means 99.9999 % of 0.04 μm Particles removed

Mini-environment Fab Floor



Cleanroom Classes



Definition of Airborne Particulate Cleanliness Class per Fed. Std. 209E

Class	Particles/ft^3				
	0.1 μm	0.2 μm	0.3 μm	0.5 μm	5 μm
M-1	9.8	2.12	0.865	0.28	
1	35	7.5	3	1	
10	350	75	30	10	
100		750	300	100	
1000				1000	
10000				10000	

3 Post Cleaning :— Post cleaning is essential after
—: Photoresist stripping, Post-CVD, Post-metallization, Post-etching

4. No IC can be fabrication without an Etching step: Two methods are used in Etching
1. Solution based etching 2. Dry Etching

Etchings are needed after oxides are formed to open windows in oxide-layer. Deep oxide etching is required for ~~at~~ creation of Isolation oxides. Echings are required for Nitride removal, metal removal and even Silicon removal for creation of Trenches.

RCA Cleaning Cycle :- Silicon wafers are cleaned with following Cycles of Steps.

	Reagent	Temp. & Time	Purpose
1	H_2SO_4/H_2O_2 1:1 to 1:4	120–150°C 10 min	(i) To Remove Organic materials; Grease, resists. (ii) Also oxidises Silicon
2	DIW Rinse		
3	HF/H_2O_2 1:10 to 1:100	Room Temp. 1 to 2 min.	Etches SiO_2 and removes impurities in this layer
4	DIW Rinse	3-5 minutes	
5.	$NH_4OH : H_2O_2 : H_2O$ 1:1:5 or 0.05:1:5 [SC1]	80 to 90°C 10 minutes Boil	(i) Removes Organic, metals (as oxides, hydroxides) (ii) Oxidises Si
6	DIW Rinse	Room Temp 5-10 minutes	

Additional Step in IMEC Process
$H_2SO_4 + O_3$ & $H_2O + O_3$ dip. after Step 1

Reagent	Temp. & Time	Purpose
7. $HCl : H_2O_2 : H_2O$ 1 : 1 : 6	80^0 to $90^0 c$ 10 min Boil	i Chlorides removed Alkali Ions Metals as Chlorides are removed ii Oxidises Si
8. DIW Rinse		
9. 1% HF treatment Followed by DIW Rinse	Room Temp 10-20 min.	Oxide is removed

10 Drying N_2 gas flow. OR IPA vapours (INTEL)

In IC Processing Most Used Reagent is
'WATER'

We need to use Ultra High Pure water.

Quality of Water : 1. Resistivity
2. Particulate Size
3. Bacterial Content.

Tap Water : (a) Dissolved Inorganic compounds of Na, Ca etc
(b) Dissolved Organic Compounds like living matter
(c) Particulate Matter : Silica particles, Paper
(d) Microbiological life
(e) Bacteria

We have

$$H_2O \longrightarrow H^+ + OH^-$$

In Equilibrium $[H^+] = [OH^-] = 6 \times 10^{13}$ /cc in Water

Diffusibity of Ion $= \frac{kT}{q}\mu$

where $\mu = zqD/kT$ is obtained from Nerst-Einstein relationship

$\therefore \mu_{H^+} = \frac{qD_{H^+}}{kT}$. We know $D_{H^+} = 9.3 \times 10^{-5}$ cm/sec

$D_{OH^-} = 5.3 \times 10^{-5}$ cm/sec

$\therefore \mu_{H^+} = 3.59$ cm²/V.sec

$\mu_{OH^-} = 2.04$ cm²/V.sec

Hence resistivity ρ of Water will be

$$\rho = \frac{1}{q \mu_{H^+} c_{H^+} + q \mu_{OH} c_{OH^-}}$$

$$= \frac{1}{1.6 \times 10^{-19} \left[(3.59 \times 6 \times 10^{13}) + (2.04 \times 6 \times 10^{13}) \right]}$$

$$= 18.5 \text{ M}\Omega \text{ cm}$$

	Tap Water	DIW
1. ρ	200 Ωcm	> 18 MΩcm
2. Electrolyte	2×10^5 ppb	< 10 ppb
3. Particulate	10^5 no/cc	< 10 no/cc
4. Organic	$10^2 - 10^5$ no/cc	< 10 no/cc

CDEEP
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