Etching in VLSI Processing

1. Wet Etching
2. Dry Etching
   - Plasma Eching
   - Reactive Ion Etching
   - Sputter etch

Films to be etched :

1. SiO_2, 2. Si_3N_4, 3. Silicon, 4. Polysilicon

§ Metals like : Al, Ti, Mo, W, Va & Copper

§ Alloys & compounds : TiO_2, TiN, Silicides of Mo, Pt

A. Wet Etching

(a) $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$

(b) $Si_3N_4 + 6HF \rightarrow H_2SiF_6 + NH_4OH$

Poly is etched in [redacted]: $HF : HNO_3 : H_2O :: 6 : 100 : 40$

(c) $HCl + H_2O$ can etch Al

$H_3PO_4 + HNO_3 + H_2O$ can etch Al.

In etching selectivity is major parameter to decide.

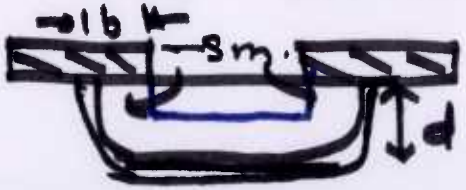
If r_1 is etch rate in film 1 and r_2 is the etch rate in film 2, then Selectivity

$$S = \frac{r_1}{r_2}$$

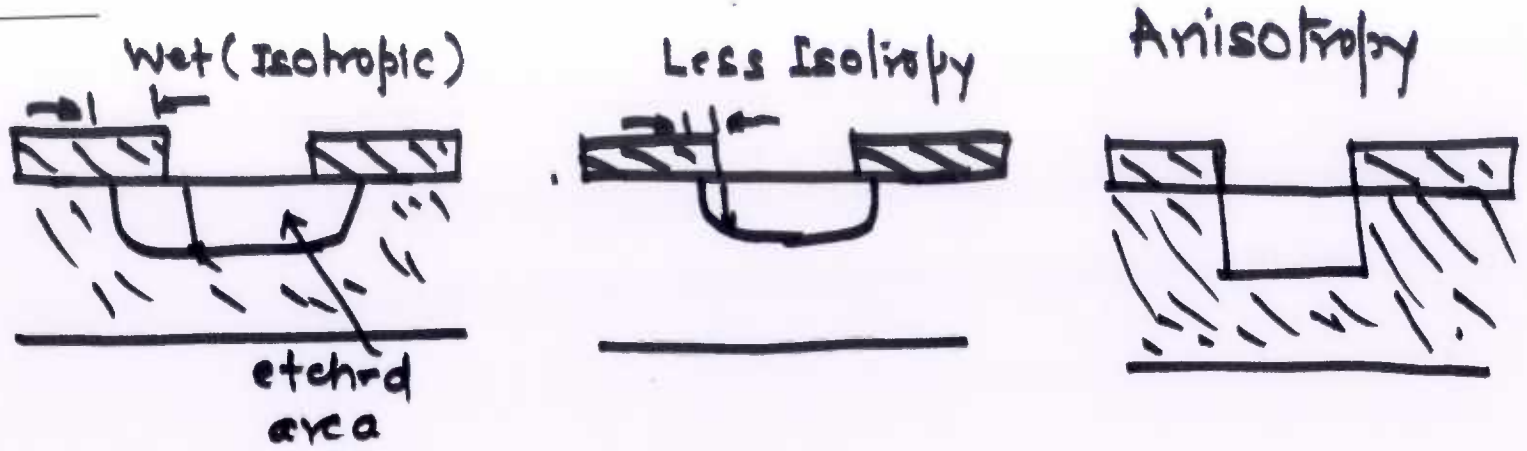
Higher the value of S, we can have ~~specifi~~ specific film etched and other not affected.

Disadvantage of Wet Etching:

Wet Etching is Isotropic in nature and hence creates unwanted etched pattern.



'b' is called Bias.



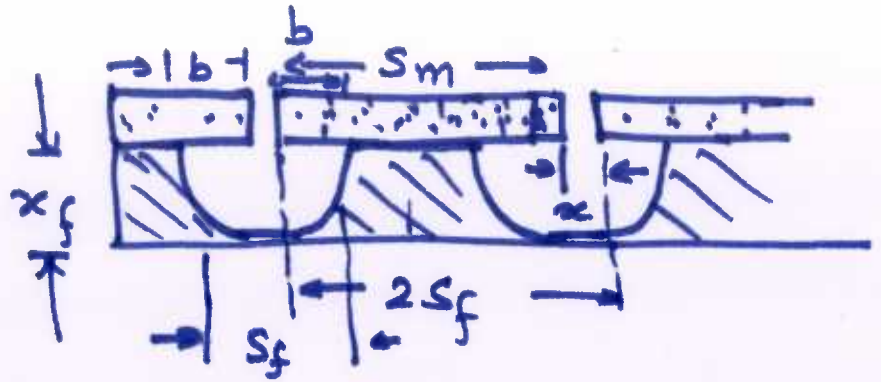
Anisotropy is defined as

$$A_f = 1 - \frac{r_{lateral}}{r_{vertical}}$$ r is Etch rate

From earlier figure if time of etching is t

then $b = r_{lateral} \cdot t$ & $d = r_{vertical} \cdot t$

$$\therefore A_f = 1 - \frac{b}{d}$$



x = Distance between Mask edges

S_m = Mask Width

① Clearly $2S_f - S_m = x$ ② $S_m = S_f + 2b$

③ $S_m = S_f + x_f (1 - A_f) \times 2$

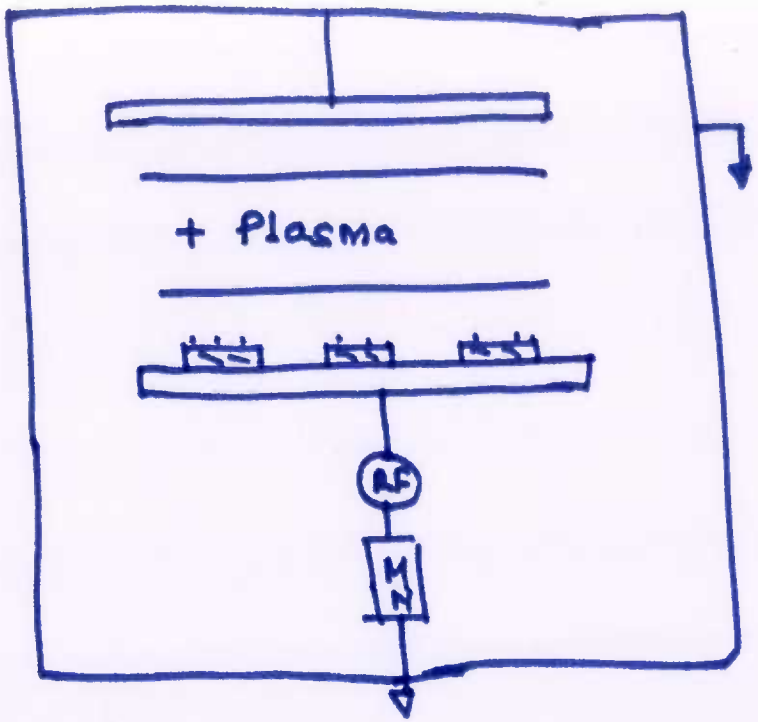
④ $A_f = 1 - \frac{b}{x_f}$ where b is Bias.
and x_f is Film thickness

or $\frac{b}{x_f} = (1 - A_f)$ or $b = x_f (1 - A_f)$

⑤ $\therefore x = 2S_f - S_f - 2x_f (1 - A_f)$

$x = S_f - 2x_f (1 - A_f)$ or $S_f = x + 2x_f (1 - A_f)$

S_f = Film width & spacing after etching



R.I.E.

RF causes ions & electrons to change their direction of motion as per field. However Ions are heavier and hence cannot move as fast as electrons. Some of the electrons are absorbed at the wafer Surface and it becomes −vely charged. Plasma has more +tive (ions) charge. The field direction is such that Reactive ions are brought to the wafer surface. This chemical etching process is directed as the field, vertically down causing Anisotropic Etching.

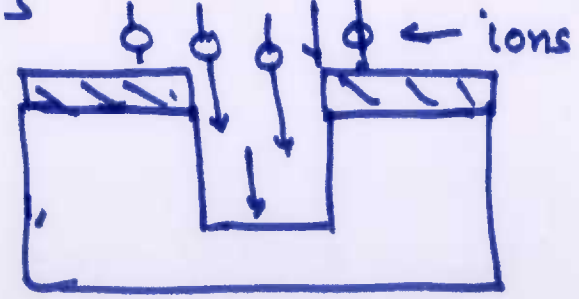
Freon or similar Florine based compound gases are used in most film etching. However other halid containing species such as Cl_2, HBr, & F.

Silicon etching is possible using nascent F created, by reaction $Si + 4F \rightarrow SiF_4$

$CF_4 + e^- \rightarrow CF_3 + F + e^-$ Dissociation

$CF_3 + e^- \rightarrow CF_3^+ + 2e^-$ Ionisation

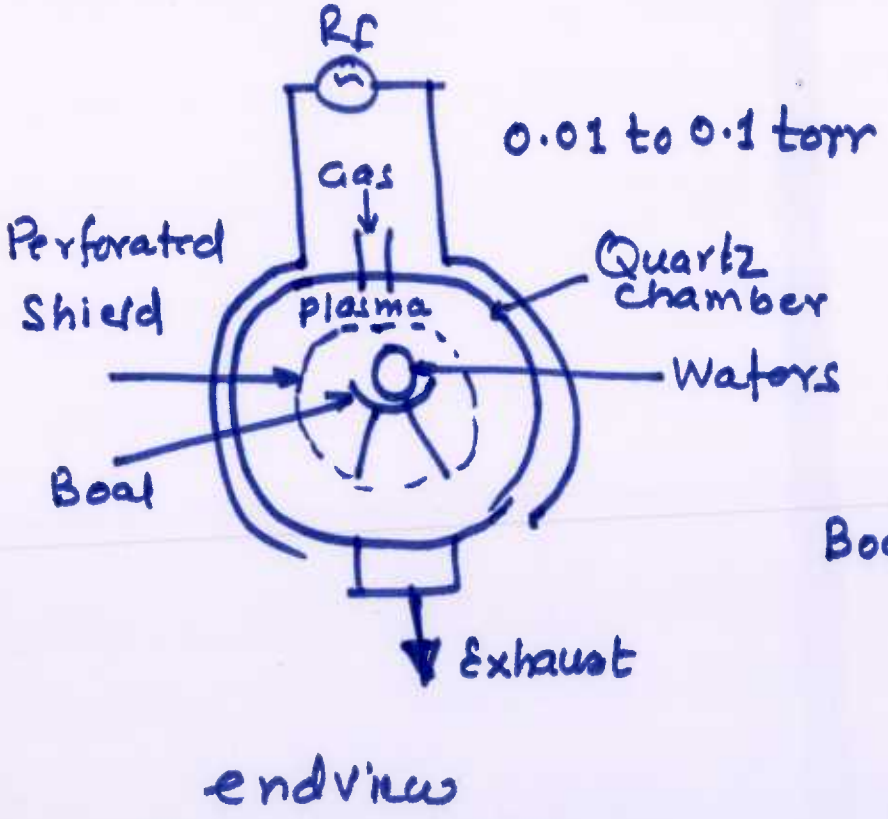
$CF_3^+ + F + e^- \rightarrow CF_4$ Recombination



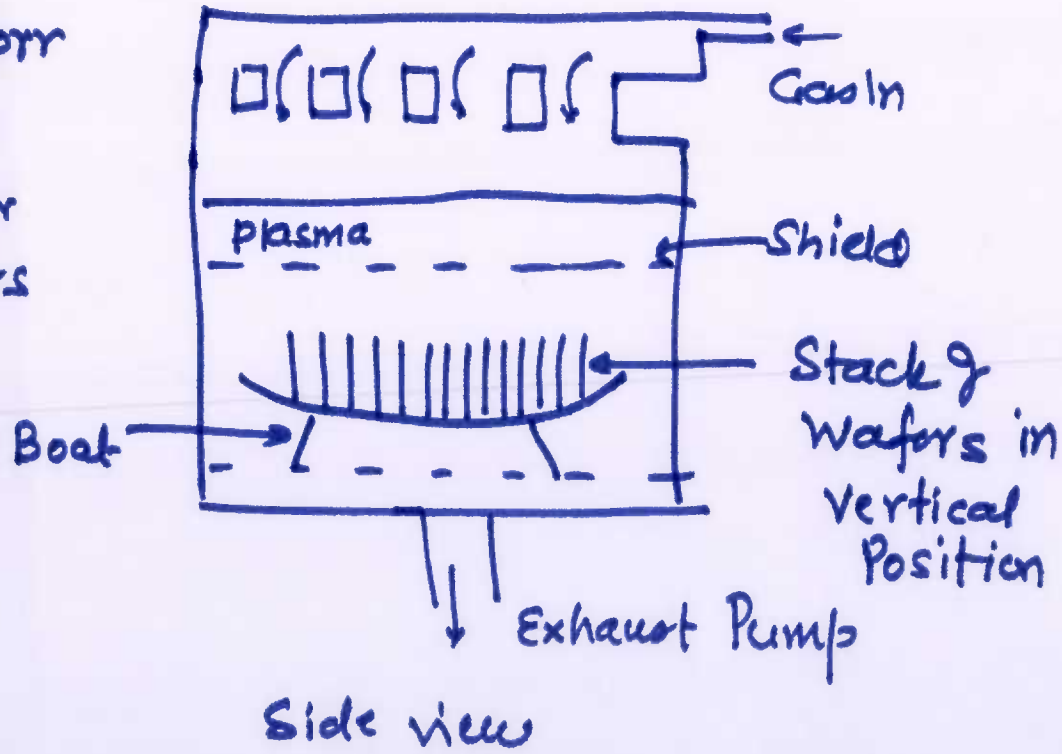
Plasma Etching : (reactive Specis of Florine used)

This is Isotropic etching but it is Dry Etching

It is used in Ashing of Resist using Oxygen Plasma



end view



Side view

Etching Models :

(i) Linear Etch Model

(ii) Saturation/Adsorption Model for (RIE)

(i) Assumption: chemical & Ionic components in Plasmaetching, independently act and superimpose each other. Then Etch rate is given by

$$\text{Etch Rate} = \underbrace{\frac{S_c K_f F_c}{N}}_{\text{Chemical}} + \underbrace{\frac{K_i F_i}{N}}_{\text{Ionic}}$$

Here F_c is chemical Flux and F_i is Ionic flux at each Point on Surface

K_f is Rate constant for Ch. Process & K_i is rate constat for Ionic Case.

S_c is sticking Coeff of chemical atoms on Surface $[0 < S_c < 1]$

& Finally N is the density (/cc) of Film material

In this model we say that vertical etching is due to both Chemical & Ionic processes. However etching in lateral direction, one can say that only chemical reaction occures as Ions Travel mostly in Vertical direction. For this case we can take $f_i = 0$

(ii) Saturation/Adsorption Model:

In this one assumes that both Chemical & Ionic processes act together. Here assumption is that neutral flux creates sites for etching. It is shown that-

$$\text{Etch Rate} = \frac{1}{N} \frac{1}{\left[\frac{1}{K_i f_i} + \frac{1}{S_c F_c}\right]}$$

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Back-End Technology

Back-End Technology in IC fabrication refers to metal layers above 1st Metal layer, which leads to Interconnects.

Interconnect layers these days are six or Seven. This needs for creation of

(i) Contacts

(ii) Vias

(iii) Intermetallic Dielectric

Current Complex Systems needs larger number of interconnects from large nodes of circuit. The success of realisation of Complex System depends on place & (route) of Devices and Interconnecting them for high performance.

An Interconnect (Metal line on Dielectric) is is like an RLC circuit or precisely a transmission line at higher frequency (Lower Technology Node). The analysis shows that the delay increases as technology scales.

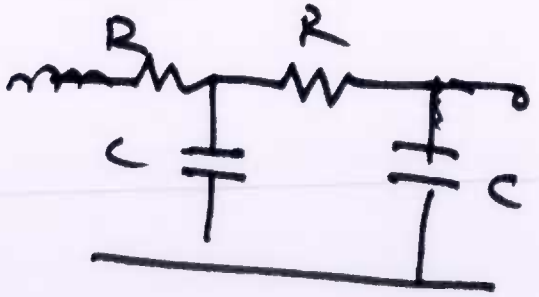
Typically even for RC delay model, the delay on a line is

$$\tau_L \propto \text{Area (chip)}$$

$$\propto \frac{1}{(F_{min})^2}$$

$$\propto K_{oxide}$$

$$\propto \rho \text{ (Resistivity)}$$



Hence for Higher Performance Circuits, this is the biggest hurdle to cross.

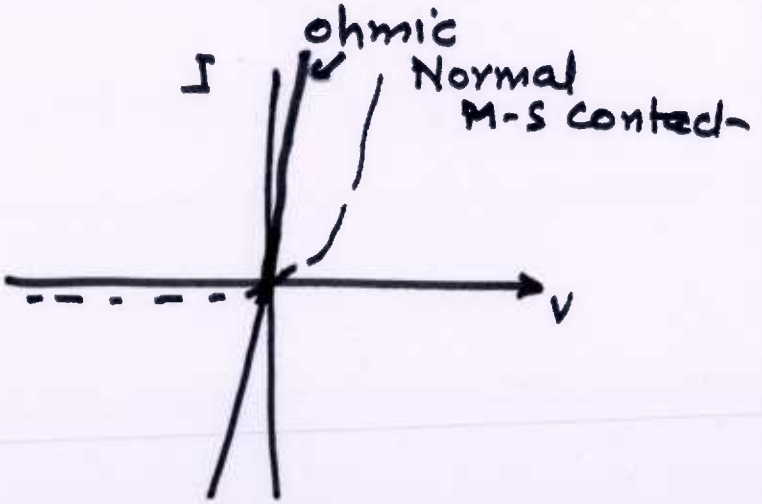
Aluminum as Contact and as Interconnect.

i Al forms a good contact with S & D.

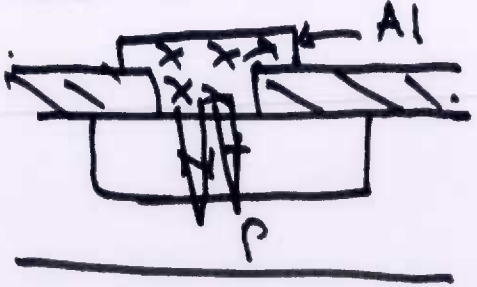
a. Al–Si alloy is formed at around 450°c

b. Al is dopant in silicon

Good contact means – ohmic Contact



Problem with Al :



(a) Junction Pitting

As Silicon has solubility in Aluminum and hence at 450°c, Silicon also diffuse through S/D towards Al. Al then finds voids and diffuse through Silicon n^+ region into substrate P. This creates spikes shorting source.

TiN layer could be used as Barrier layer between Al and Si (S&D regions)

(ii) Stress Effect: Due to compressive Stress developed by Al line running over SiO_2 layer, at times Hillocks are formed due to grain-boundary diffusion.

This can break the interconnect.

(iii) Third Problem is due to Electromigration (Discussed earlier)

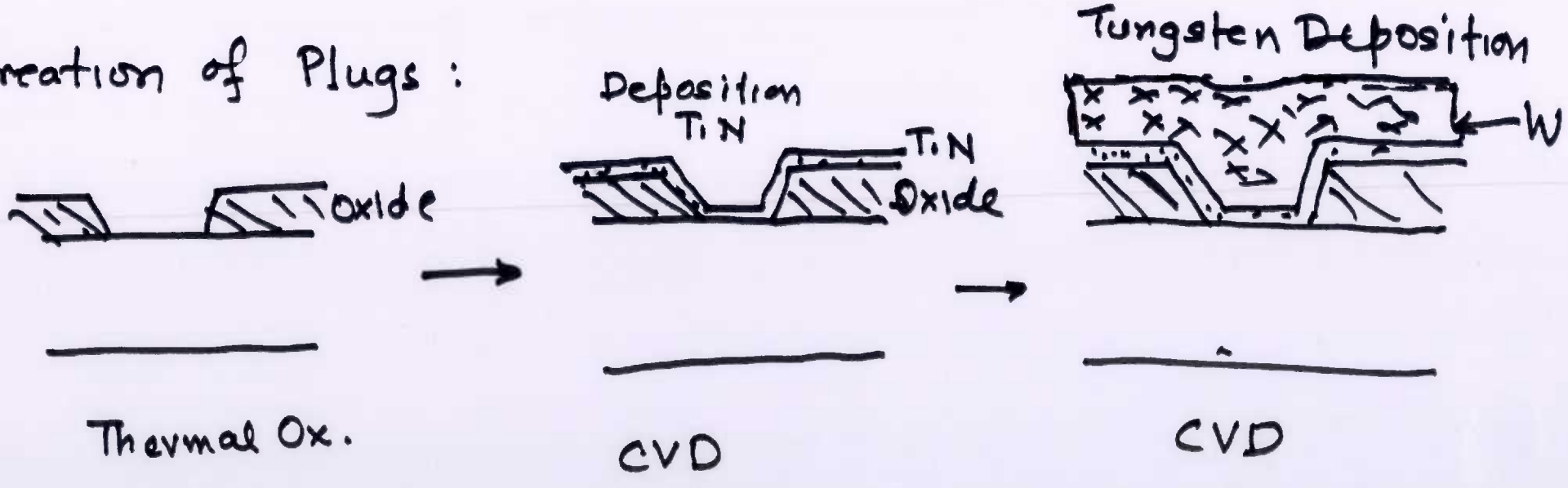
(B) Copper Technology for Interconnect.

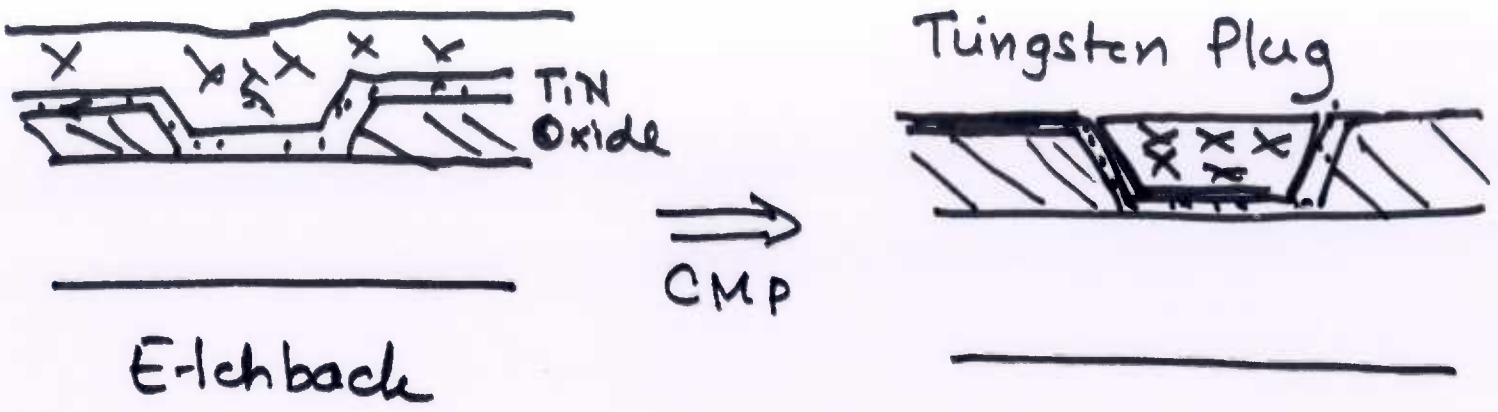
For lower resistance interconnect / length, Al is replaced by Copper in upper layers of Interconnects. Copper is a trap giving impurity in Si, and hence needs separation between itself & Silicon. This is called Cladding.

TiN, or Tantalum based alloys or Vanadium oxides are used as Cladding layers.

The Copper interconnect process was invented by IBM and Texas Instrument around year 1998. This speeded up the Circuit by almost $1\frac{1}{2}$ times with the same technology & architechures.

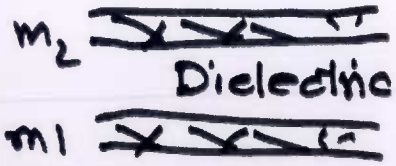
(9) Creation of Plugs :





This process is called Damascene Process.

(D) Intermetallic Dielectric : Two metal layers (Cu or Al) are separated by Dielectric layer called IMD. This structure acts like Capacitor.



Thus signal on m_1 can get connected to m_2 through this capacitor. To avoide cross-talk, Z should be v. large. However with increase of frequency of opelation of circuits, Z actually reduces.

$$C = \frac{\epsilon A}{t}$$

$$Z = \frac{1}{j\omega C}$$

Further as interconnects run longer, the 'Area' too increases for capacitor. This too then reduces 'Z'.

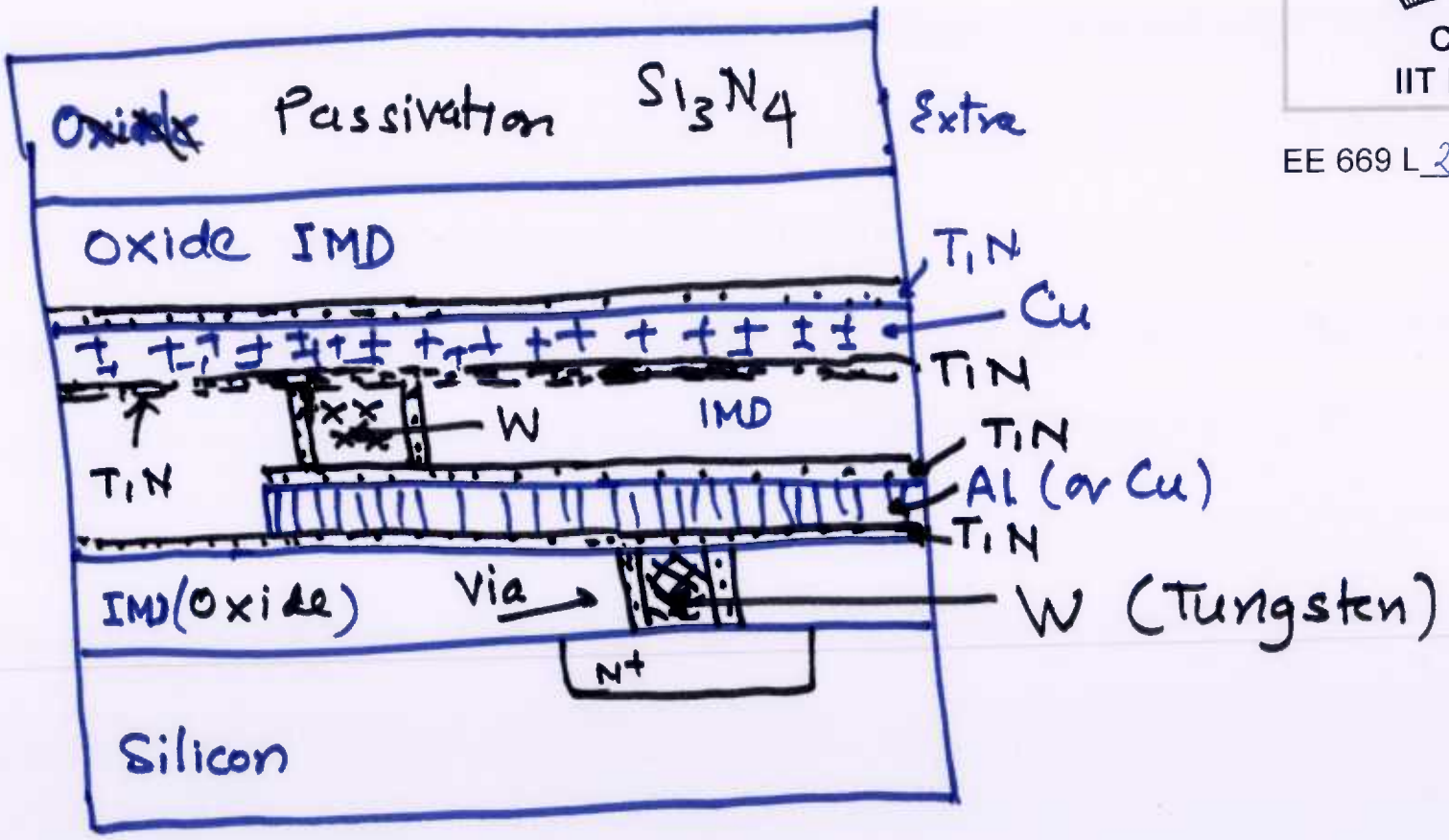
Hence to avoid cross-talk, or to increase Z at operating frequency we have two options:

(i) Increase Oxide Thickness. But it leads to
- More Non-planer structure
- Deeper Vias (Reliability Issue)
- Non Filling of Vias by metal

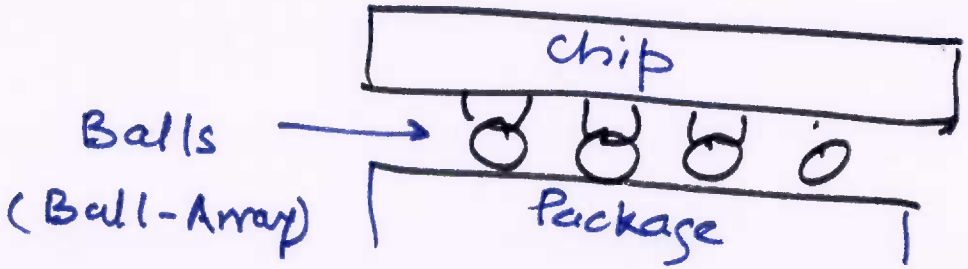
Hence this option is limited option.

(ii) Second option is to use Dielectric with lower ϵ ($K\epsilon_0$)
HSQ (Hydrogen silsequioxane) with K of 2.8 is better than SiO_2. Organics like Fluoro-polymers can give $K = 1.8$. Porous SiO_2 can give K of 1.2 - 1.8. Air Bridge: K = 1

Typical two layer Interconnect with connection from layer 2 to S/D Silicon



Packaging



Flip Chip Ball Bonding