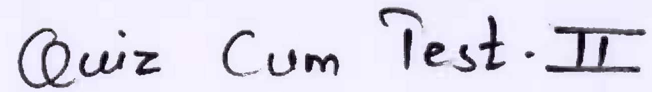
L-23 ~~slide~~

Slide: 01



Quiz Cum Test-II

30th October 2014

Time: 8·45 PM to 10.00 PM

Venue: GG 001 and GG 002

Course: "After Mid. Sem till 29th October

"NO" SHEET during Exam

Polysilicon Gate Realization

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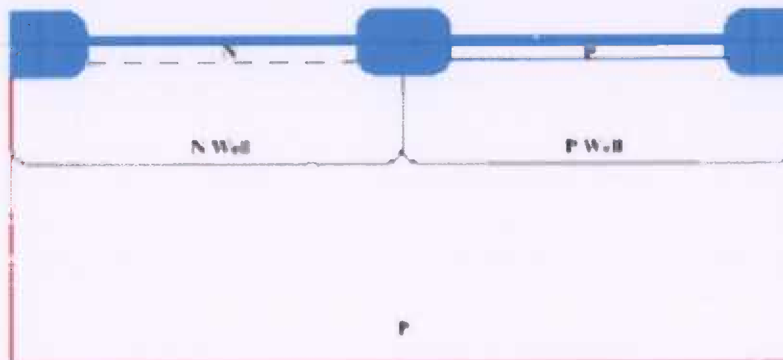
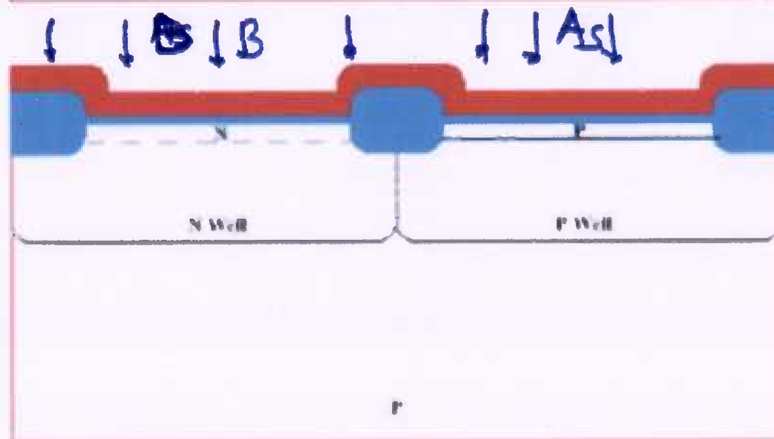
Gate Stack Formation



- Etch back thin oxide and **grow clean gate oxide** ~ 5 nm, which can be grown at 800°C in ~ 1 hr.

Nitrided oxides are typical today, and alternative high-K dielectrics are also being considered. for sub 90 nm, Node

Dry Oxidation



- LPCVD **polysilicon gate deposition** (~0.1 microns). Either masked or unmasked polysilicon doping implant is then performed (target dose such that final average poly doping is > 10^{20} cm^{-3}).

$R_s \simeq$ 10 - 20 ohm/□

Doping of Poly.
1. In Situ during Poly deposition
2. Solid State Diff.
3. Implant

Gate Delineation

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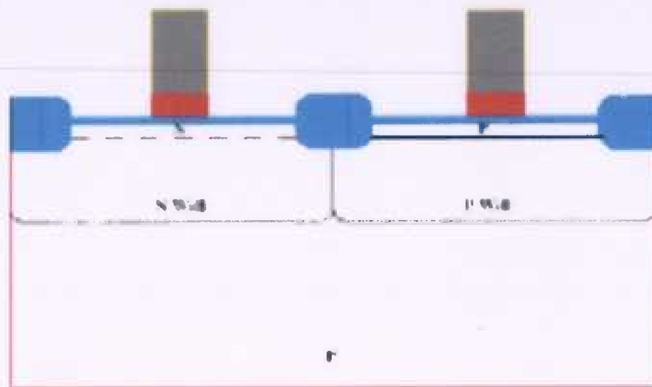
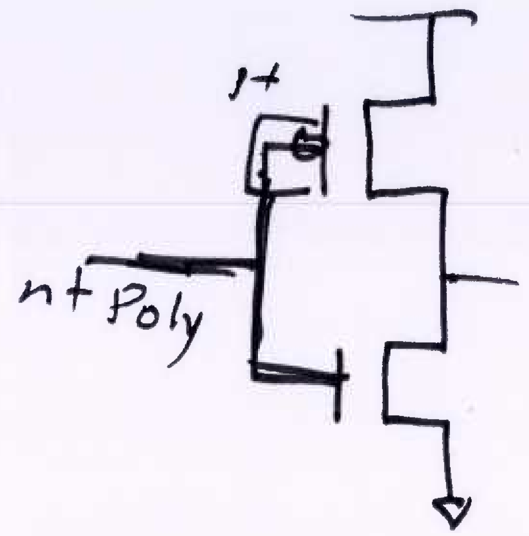
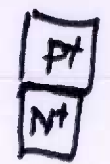


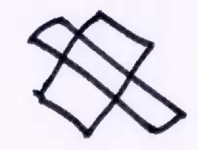
• **Gate etch**: Mask #6 is used to protect the MOS gates. The polysilicon is plasma etched using an anisotropic etch which stops on the underlying oxide.

Process option: **gate re-oxidation** (to improve reliability in very thin gate oxide devices). Must be done carefully to avoid formation of non-uniform gate oxide thickness:

K. Rim, Ph.D. thesis, Stanford Univ.





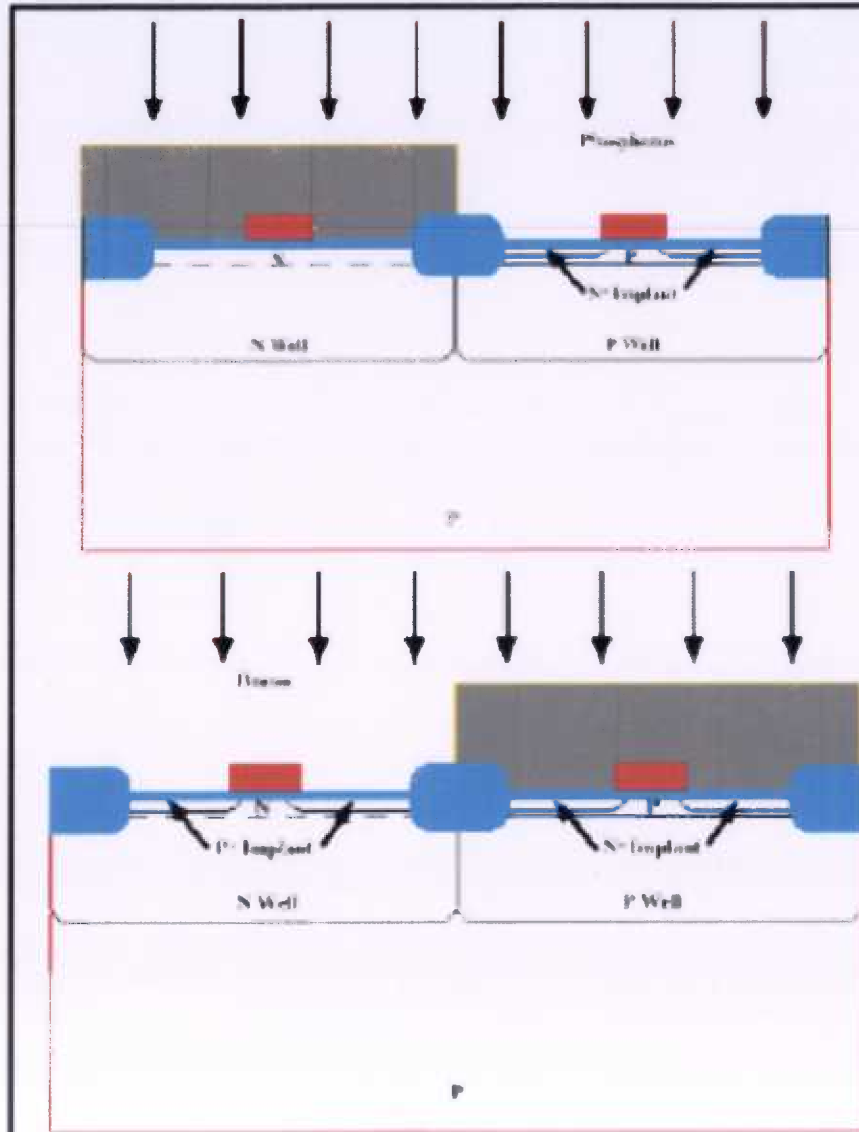


R ∧ C → Tran.

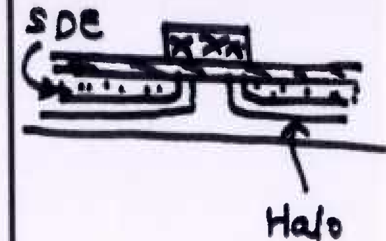
L23-S-05

S/D Extensions for SCE reduction

EE 669 L 22 / Slide 18



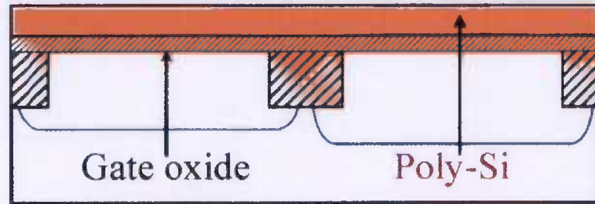
• **NMOS S/D Extension formation:** Original concept was Lightly Doped Drain (LDD) to help deal with hot electron effects. Today, the S/D extension serves to mitigate short channel effects. Mask #7 protects the PMOS devices. An As+ implant forms the LDD regions in the NMOS devices.



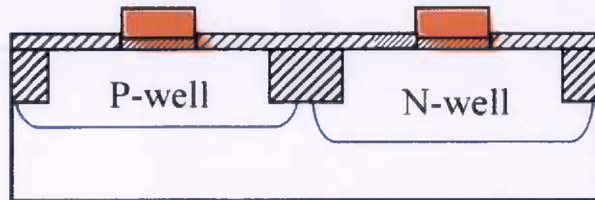
• **PMOS S/D Extension formation:** Mask #8 protects the PMOS devices. A B^+ implant forms the LDD or extension regions.

Lec No - 23 Slide - 6

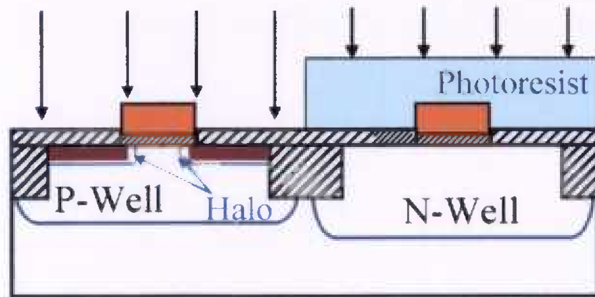
CMOS Fabrication



4 Gate formation:
- Clean silicon surface
- grow gate oxide
- deposit poly-Si gate electrode.

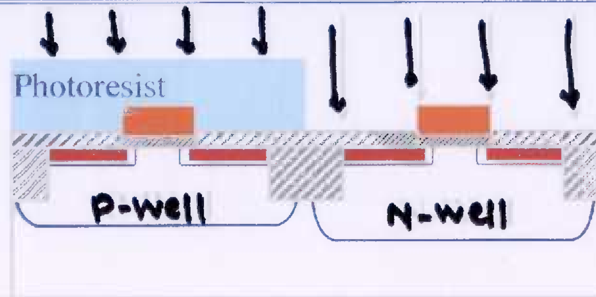


5 Mask #4: Gate definition
- etch poly-Si
- etch oxide
- grow masking oxide.



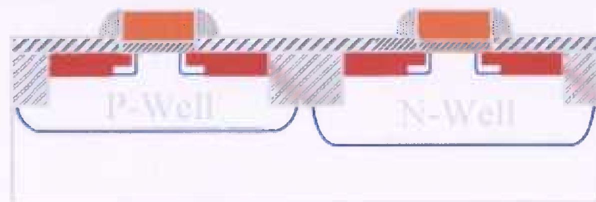
6 Mask #5: N+ source / drain extension (SDE) and p-halo:
- As SDE implant
- B/BF2 halo implant
- clean.

Halo

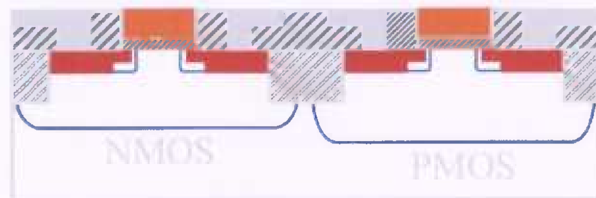


7. Mask #6: P+ SDE and n-halo:
   - B/BF2 SDE implant
   - As/Sb halo implant
   - clean.

p+ implant for S&D Extension
n - halo implant



8. Deep s/d (DSD) formation:
   - spacer deposition and etch
   - Mask #7 - N+ DSD
     - As implant
   - Mask #8 - P+ DSD
     - B/BF2 implant
   - dopant activation (RTA).



9. Interconnection:
   - Mask #9- contact opening
   - Mask #10: define metal.

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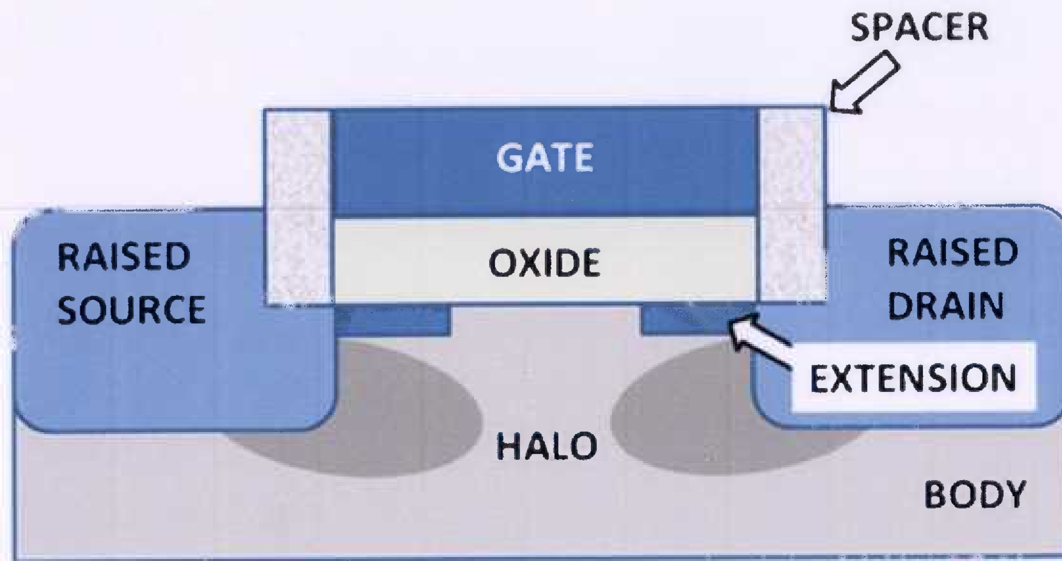
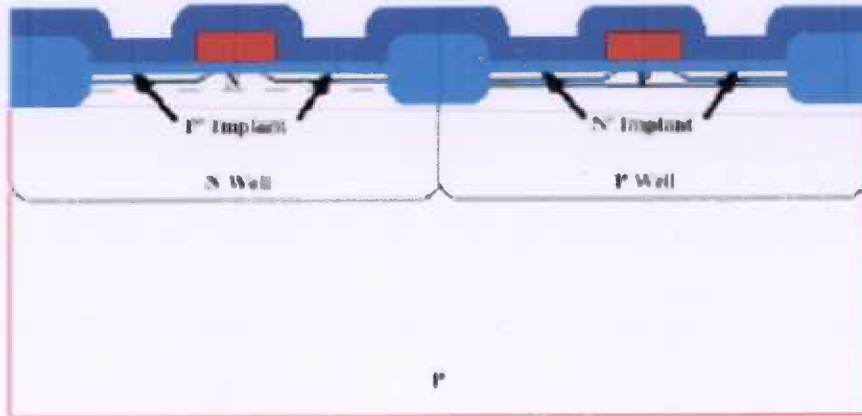

SPACER
GATE
OXIDE
RAISED
SOURCE
RAISED
DRAIN
EXTENSION
HALO
BODY

Sidewall Spacer creation

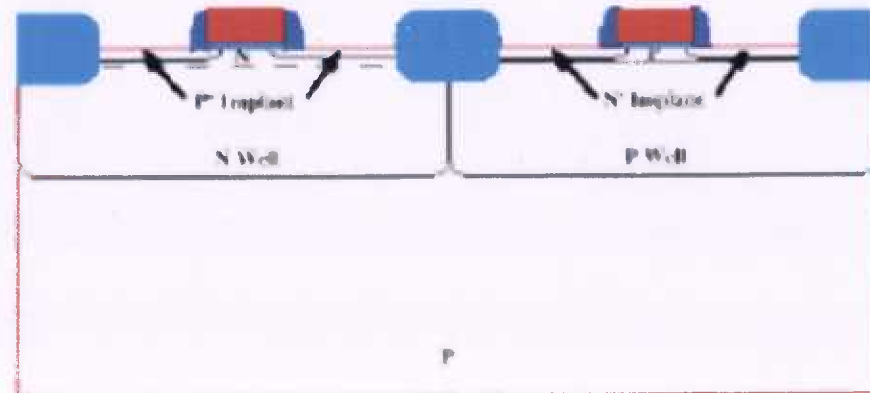


- **Sidewall spacer formation (oxide):**

A conformal layer of SiO_2 is deposited (typically ~ 0.1 to 0.25 microns thick) LPCVD Process.

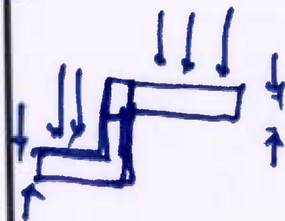
$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_2Cl_2 + N_2O \rightarrow SiO_2 + 2N_2 + 2HCl.$$



- **Sidewall formation:**

Anisotropic etching leaves behind "sidewall spacers" along the sides of the polysilicon gates.



Deep Source & Drain Formation

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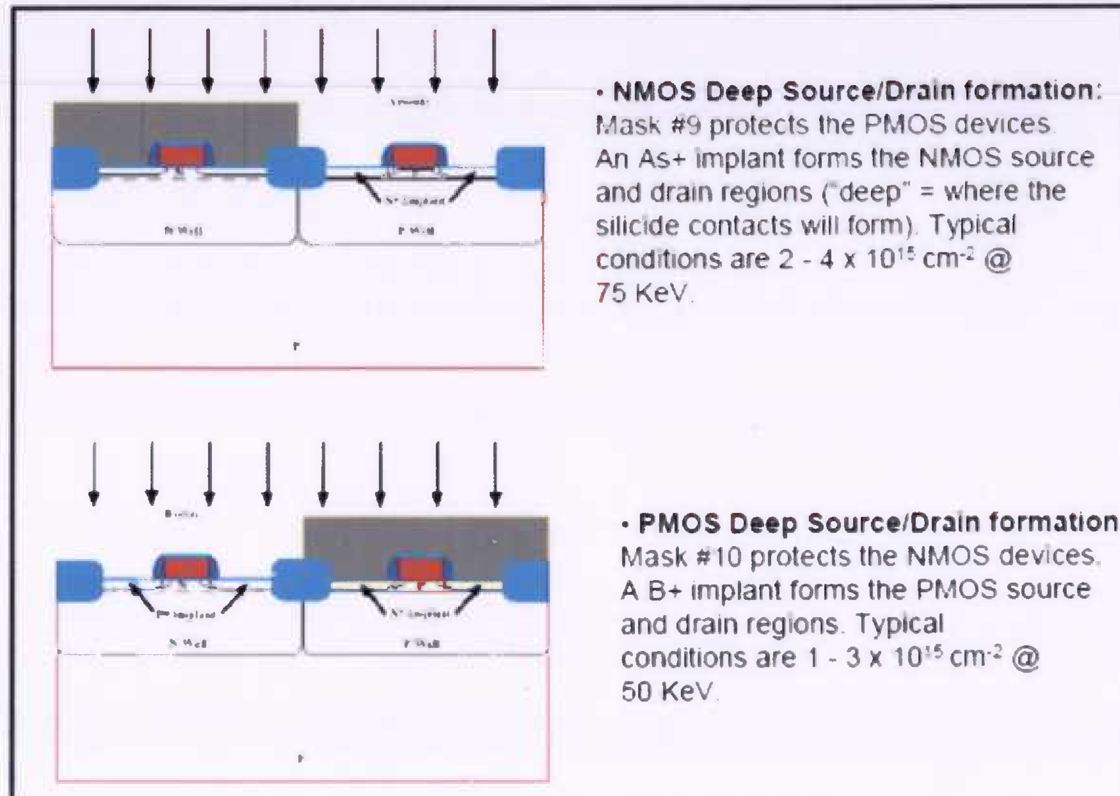
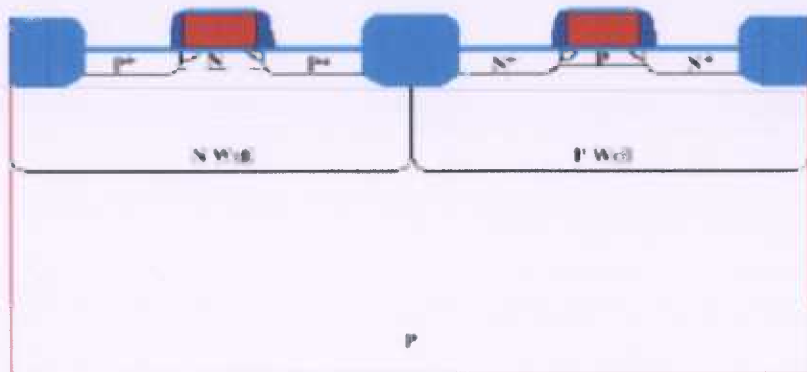
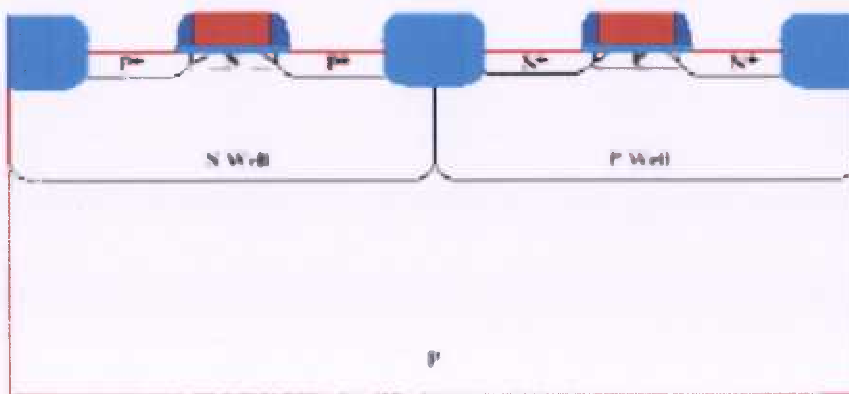


Source & Drain Contact windows



- **Final anneal**: High temperature drive-in activates the implanted dopants and diffuses junctions to their final depths. Typical conditions: 30 min. @ 900C or 1 min. RTA at 1000C.



- **Contact formation:** Unmasked oxide etch (HF dip) opens regions where contacts will be made to the Si and polysilicon.

Titanium Silicide contact to Source and Drain And Titanium Nitride Barrier creation

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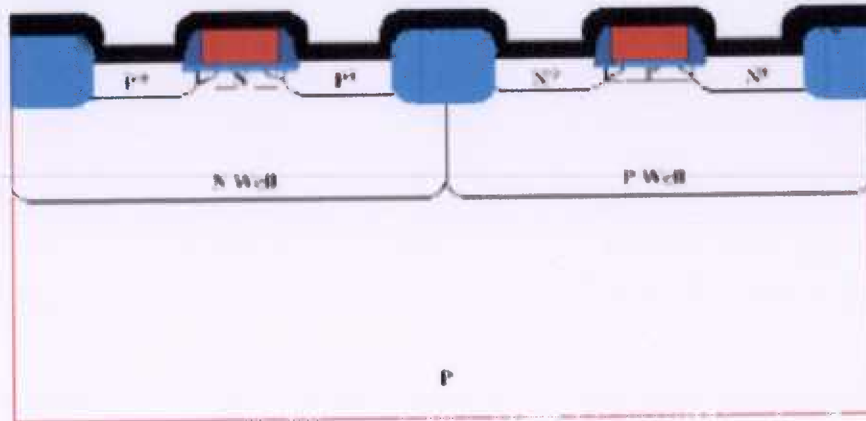
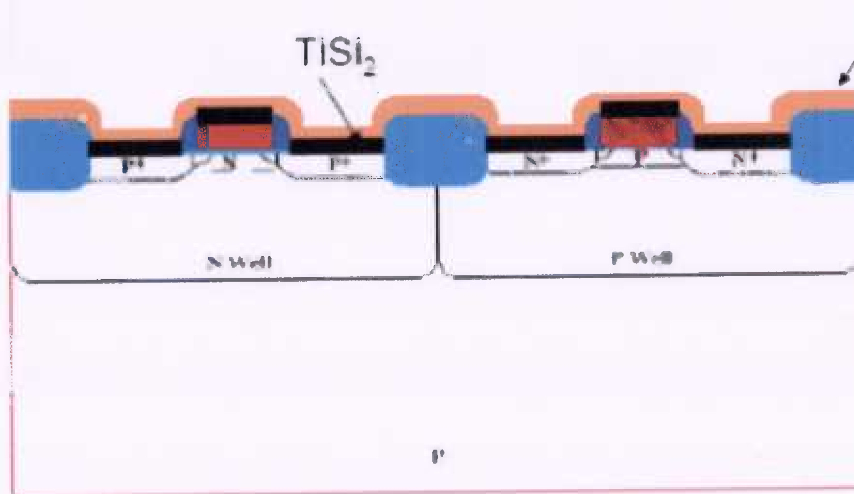


- Ti is deposited by sputtering



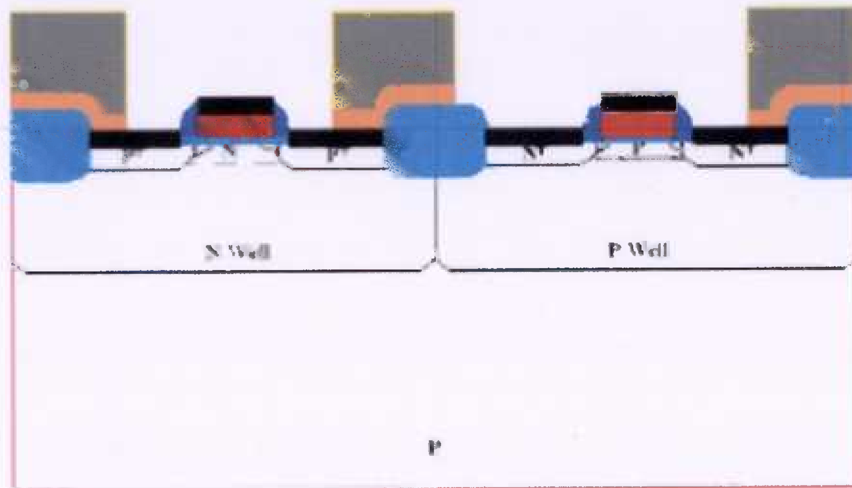
TiN → good conductor for Local interconnect

- Ti is reacted using RTA, in an N_2 ambient, forming $TiSi_2$, and a layer of TiN on top. Typical formation: 1 min. @ 600 C. - 700°C

In formation of $TiSi_2$, some Silicon is consumed. Hence S & D junction should be deep enough, to allow this Silicon consumed.

$TiSi_2$ is a good conductor and gives Low contact resistance with S&D regions

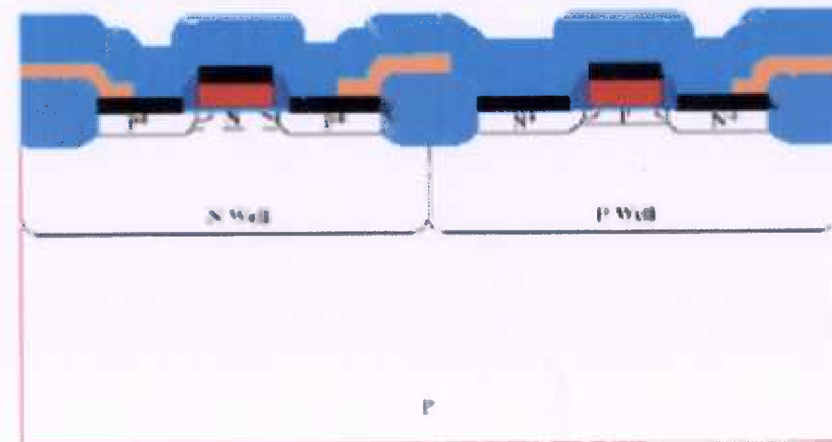
Local Interconnect to Multilevel Metal



- **Local interconnect**: Mask #11 is used to pattern the photoresist. The TiN is etched in $HN_4OH:H_2O_2:H_2O$ (1:1:5).

All TiN must be removed from the sidewall spacers.

"Front-end" is over



- **Multilevel metal formation**: A conformal layer of oxide is deposited by LPCVD (~ 1 micron). This is sometimes a phosphosilicate glass, rather than more silicon dioxide.

Sometimes glass could be Borophosphosilicate Glass as well.

BACK-END Processing Starts

Ph → Na^+
B → Glass Floco.

CMP Planerization of Deposited Oxide and Via creation for W-stub

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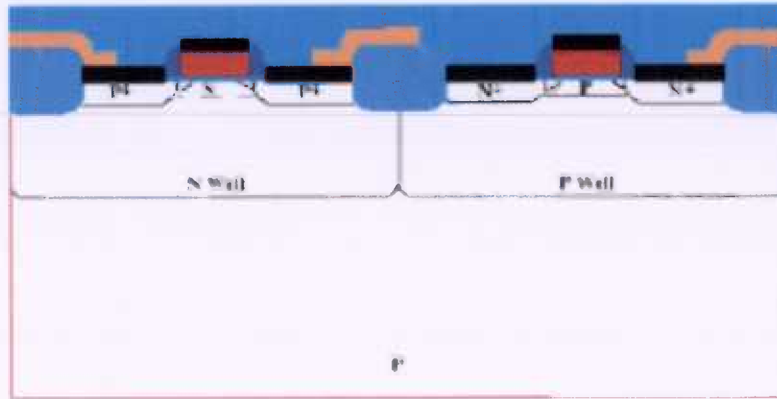
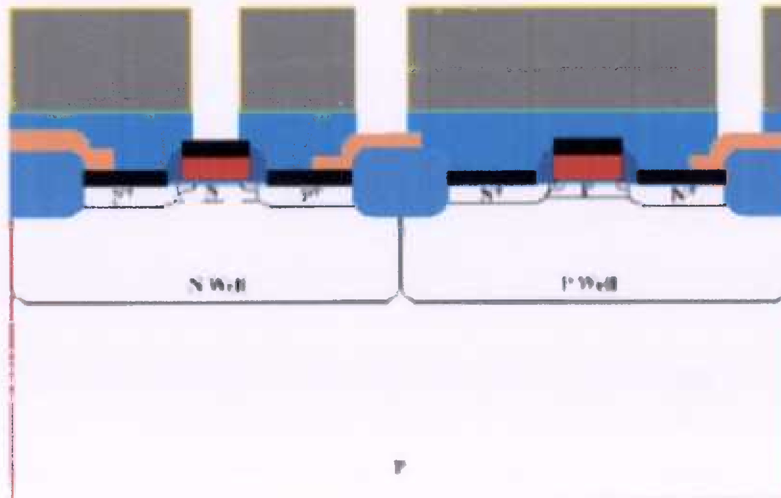


- Chemical mechanical polishing (CMP) is used to planarize the wafer surface.

High Ph-Value Silica Slurry is used for CMP.



- **Contact hole definition:**
  Mask #12
  is used to define the contact holes.
  The oxide is etched down to the TiN layers to be contacted.

Deposition of TiN Barrier and Tungsten for Stub Creation

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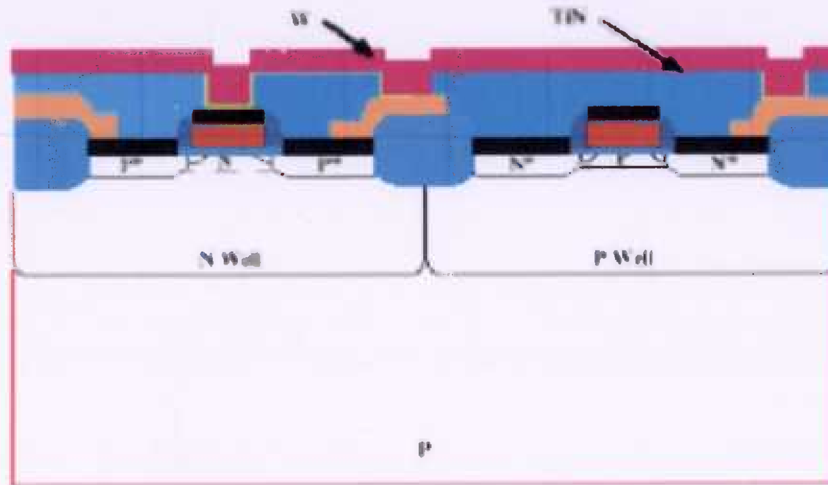
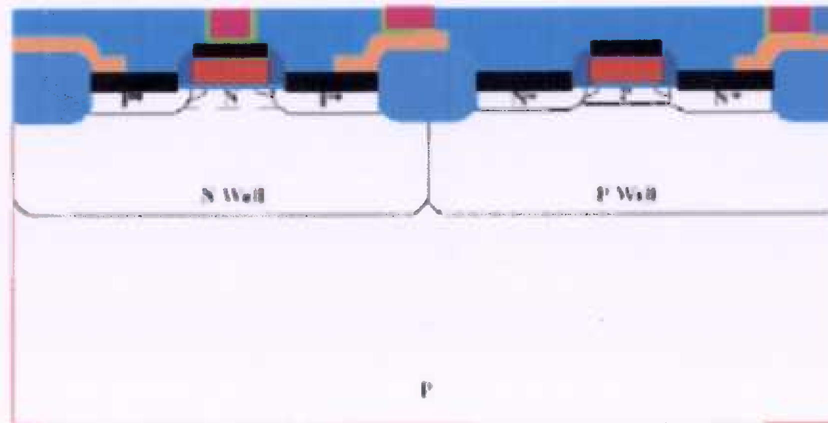


TiN has good adhesion with SiO_2.

- Thin TiN barrier layer deposited by sputtering (~ few hundred Angstrom), followed by tungsten (W) CVD deposition.

$$WF_6 + 3H_2 \rightarrow W + 6HF$$

TiN is thin layer of 100 Å or equivalent order.



- CMP is used to planarize the wafer surface, completing the damascene process.

W-Plugs

First Level Global Interconnect Metallization

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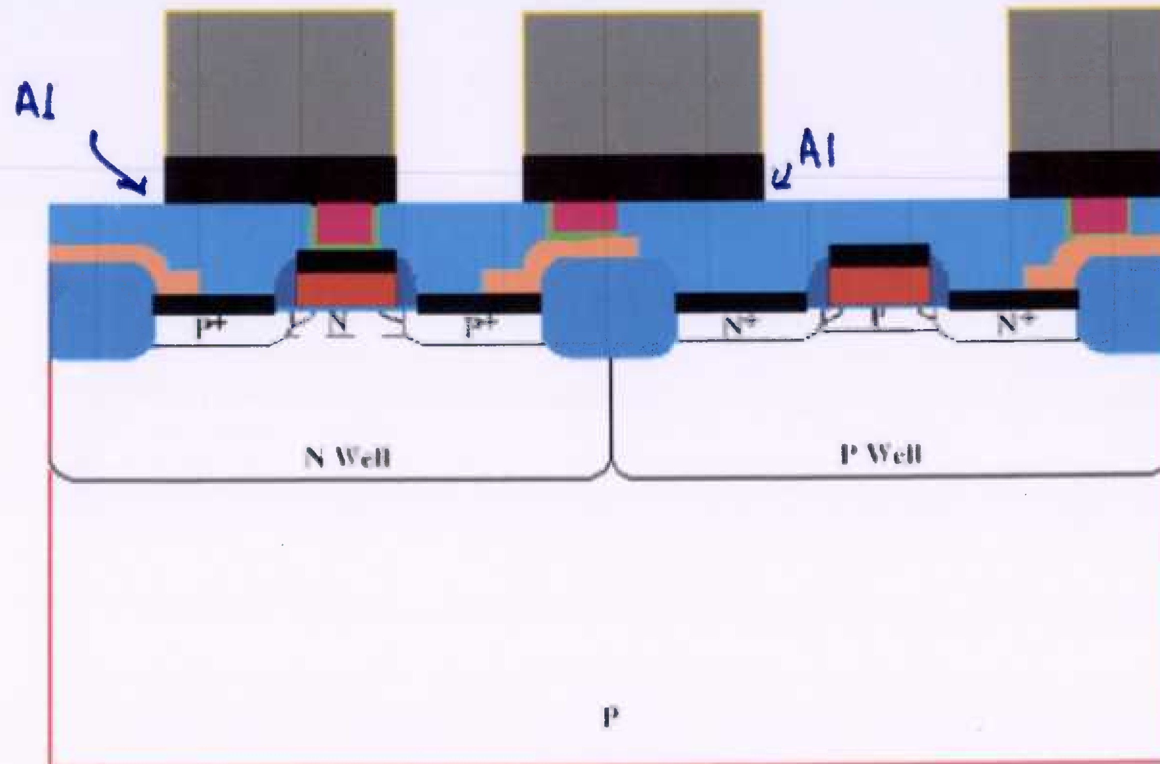
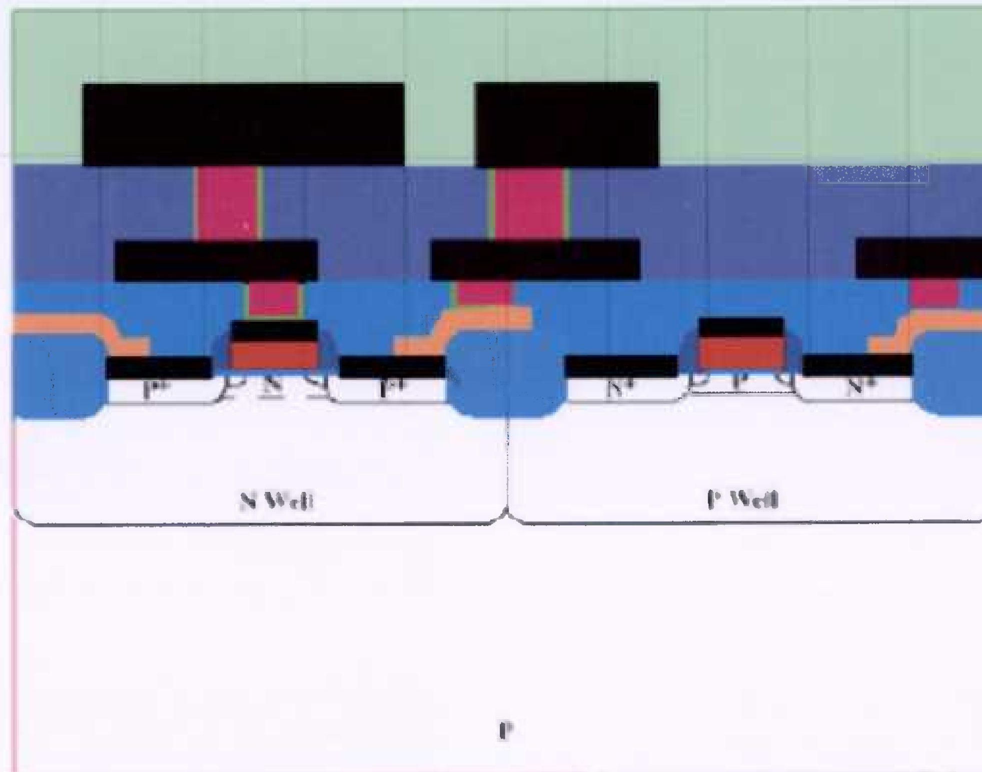


- **First level metal:**
Al is deposited on the wafer by sputtering. Resist is applied and mask #13 is used to define the first level of metal patterns. The Al is then plasma etched.

Second Level Metallization and ahead

Final Structure



• **Second level metal**: deposited and defined in the same way as Al level 1. Mask #14 is used to define contact vias and Mask #15 is used to define metal level 2. A final passivation layer of nitride is deposited by PECVD and patterned with Mask #16.