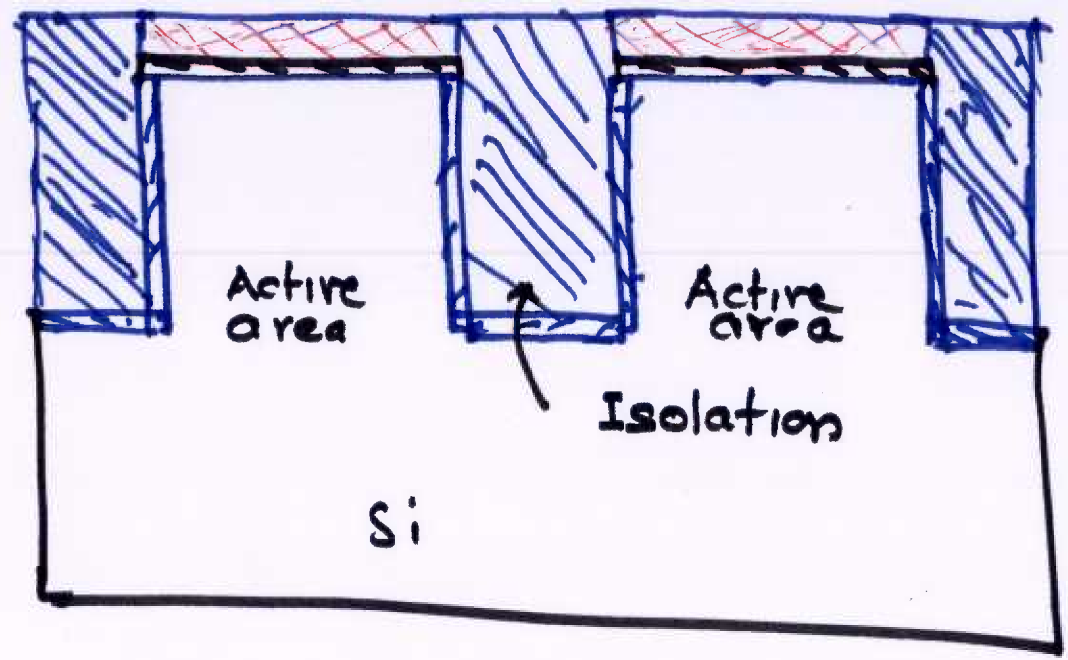
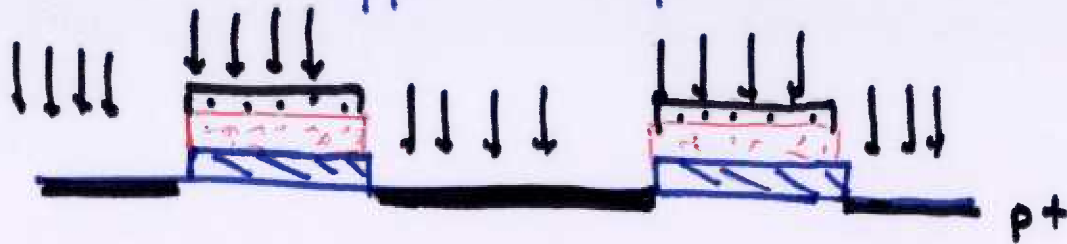
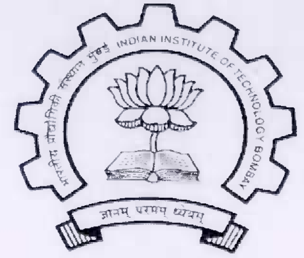
EE 669 L 31 / Slide 20



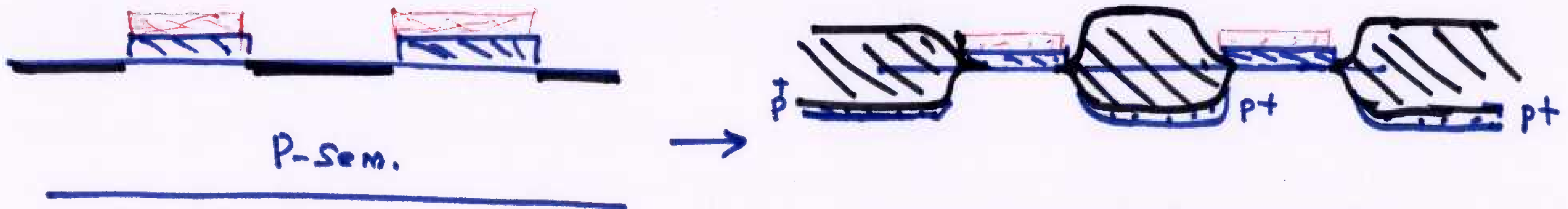
Recessed Trenched Oxide Isolation (STI)

Channel Stopper Implant





LOCOS PROCESS after Implant & removal of Resist.



$$V_{TF} = 2\phi_F + \phi_{ms} - \frac{Q'_{ox}}{C'_{ox}} - \frac{Q'_B}{C'_{ox}}$$

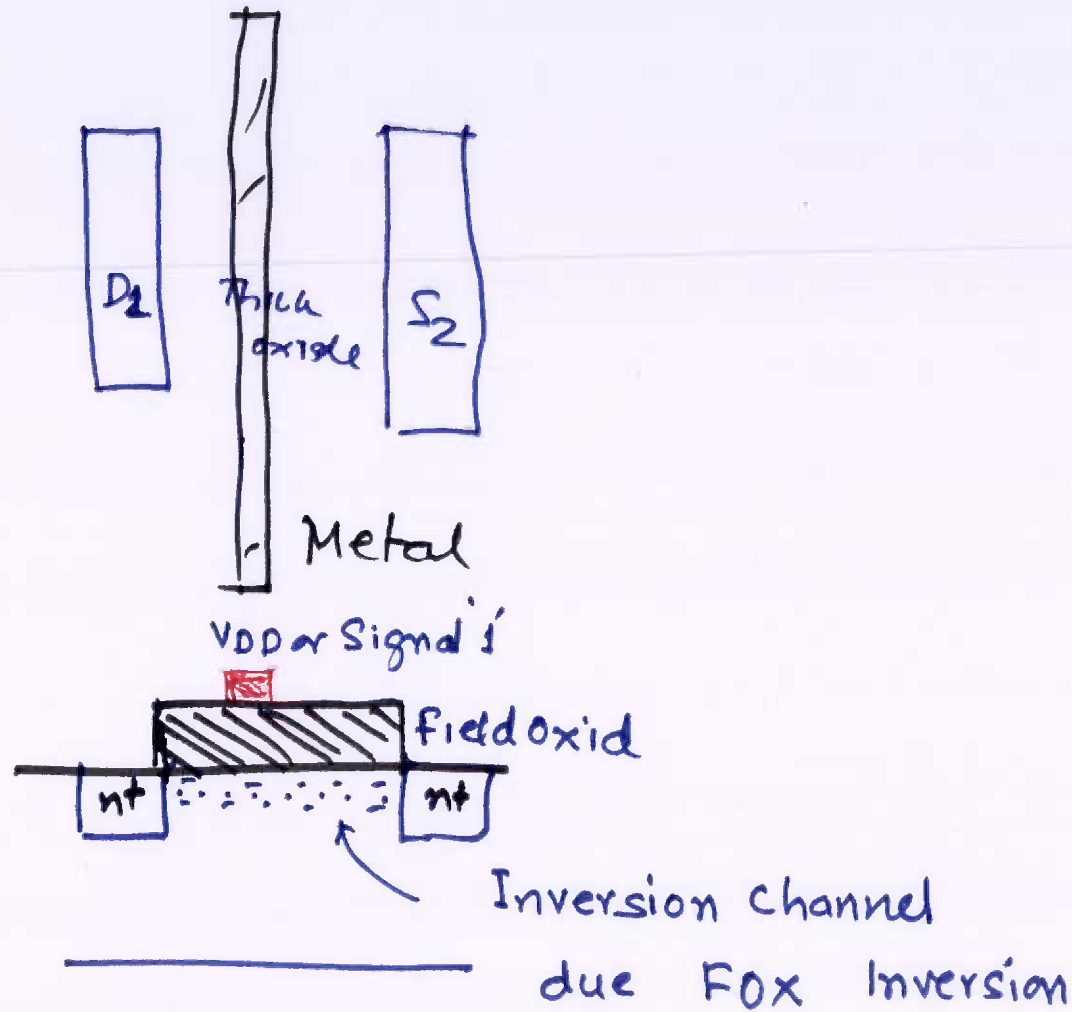
$$Q'_B = Q_B + Q_{implant}$$

$$Q_B = +q N_a x_{dmax} \quad (\text{P-Sub})$$

$$\therefore \Delta V_{TF} = -\frac{Q_{implant}}{C'_{ox}}$$

$$V_{TF} = V_{TF0} + \Delta V_{TF} \qquad C'_{ox} = \frac{\epsilon_{ox}}{t_{FOX}}$$

NMOS :



CMOS Process steps

EE 669 L 22 / Slide 4

Acknowledgements

Most of the PPTs used here are taken from

Work of Prof. Jim Plummer of

Stanford University .

His book on “Silicon VLSI Technology” is being used as one of the Text Books for the Course of

EE 669:VLSI TECHNOLOGY

Similar slides are also available from the course PPTs of VLSI Technology, a Graduate Course offered by Ms. Hoyt

At

Massachusetts Institute of Technology, Cambridge, USA

--------A.N.Chandorkar, IIT Bombay, Mumbai, INDIA

July to November 2014

Standard 16-Mask CMOS Process

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EE 669 L 22 / Slide 5

2005 International Technology Roadmap for Semiconductors (ITRS)

- A: Starting Material
- B: Isolation
- C: Well Doping
- D: Channel Surface (Preparation)
- E: Channel Doping and Channel Strain
- F: Gate Stack (Including Flash) and Spacer
- G: Extension Junction and Halo
- H: Contacting Source/Drain Junction
- I: Elevated Junction and Contacts
- J: Premetal Dielectric
- K: DRAM Stack/Trench Capacitor & FeRAM Storage

Figure 55 Front End Process Chapter Scope

From "Front-end Processes" (FEP) Chapter, Downloaded 9/5/2006 from

http://www.itrs.net/Links/2005ITRS/FEP2005.pdf

Overall Structure of CMOS

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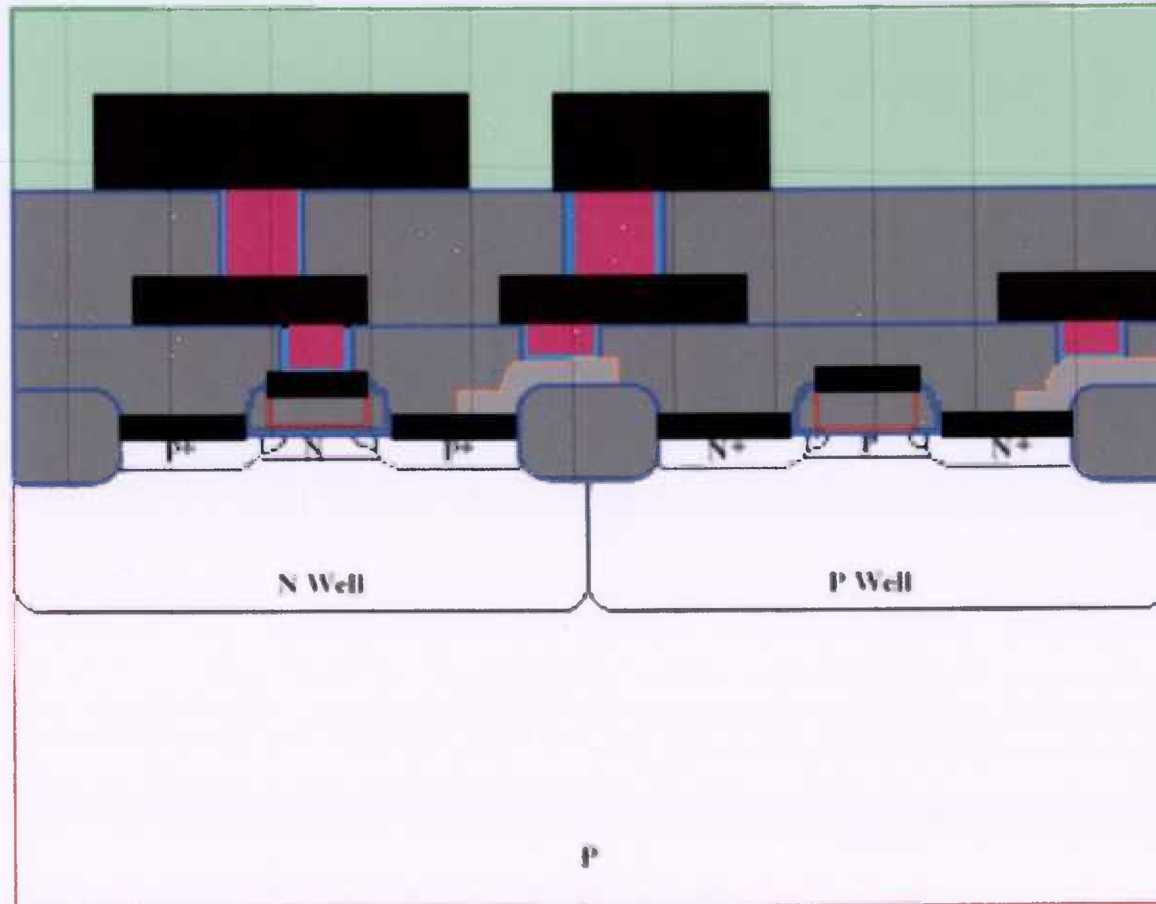
Schematic Cross Section of a Modern Silicon IC



(only two levels of wiring shown, for simplicity)

Two Level Metal Interconnect CMOS

S G D S G D
P+ N P+ N+ P N+
N Well - PMOS Substrate
P Well - NMOS Substrate
P

• Final result of the process flow described here.

Step-I :"Active Area" Processes

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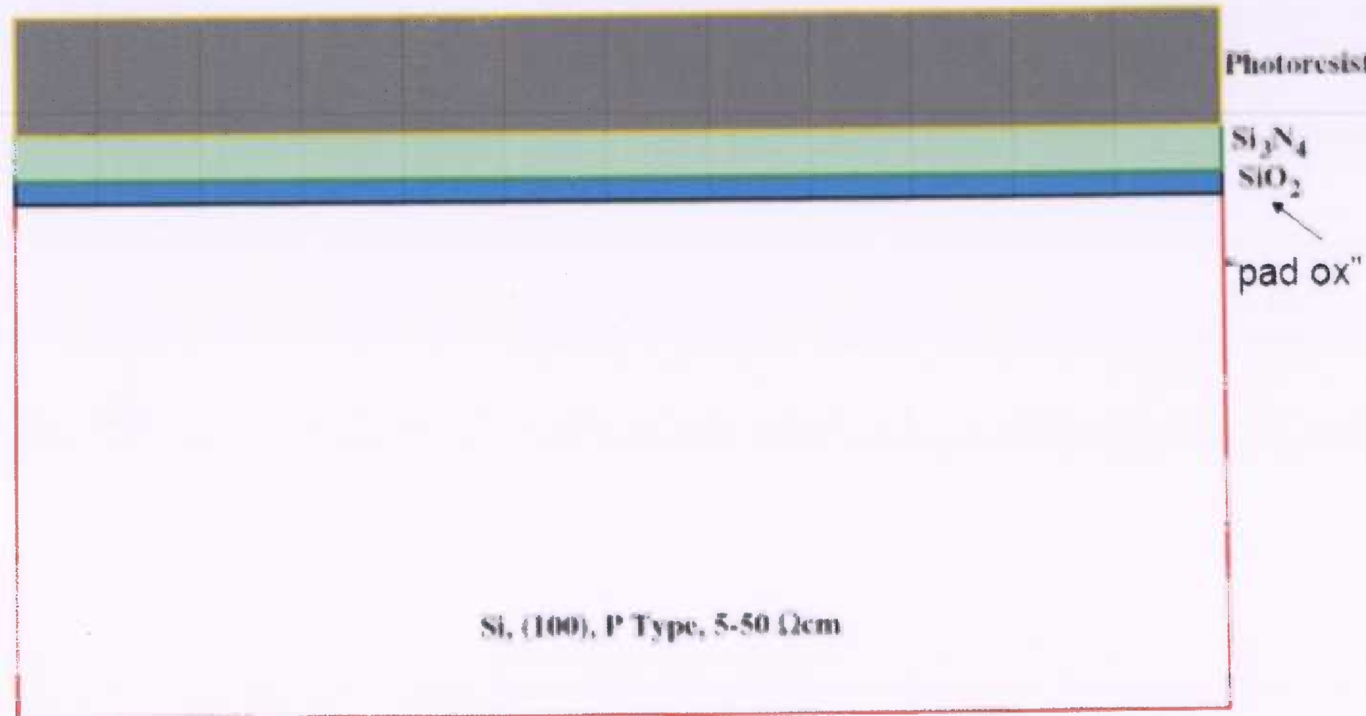

- Substrate: moderately high resistivity, (100) Si, p-type
- **Active region formation**: wafer cleaning, thermal oxidation (~40 nm), silicon nitride deposition (LPCVD) ~ 80 nm, photoresist coat (~0.5 - 1 micron)
- LPCVD Si_3N_4 is under tensile stress; compressive stress of thermal SiO_2 helps to balance this to reduce the stresses in the substrate (defect formation)

Active Area Delineation

Resist

P

- Mask 1 patterns the resist. The nitride is then dry etched to protect the active areas.

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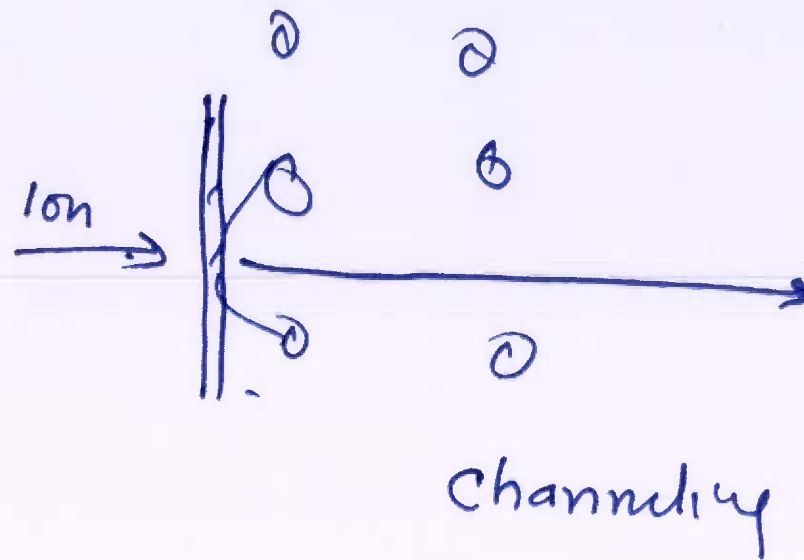
Ion
Channeling

LOCOS and P-well creation

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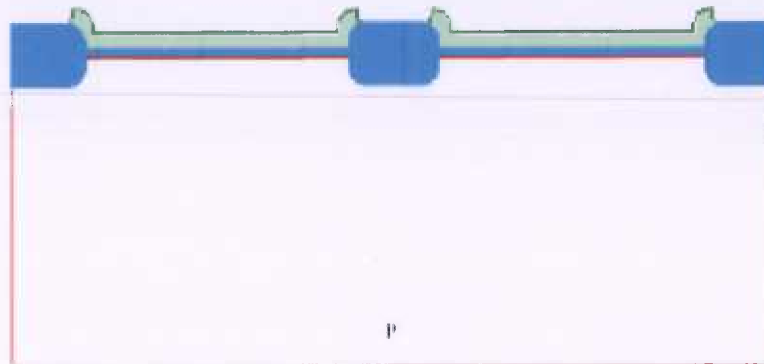
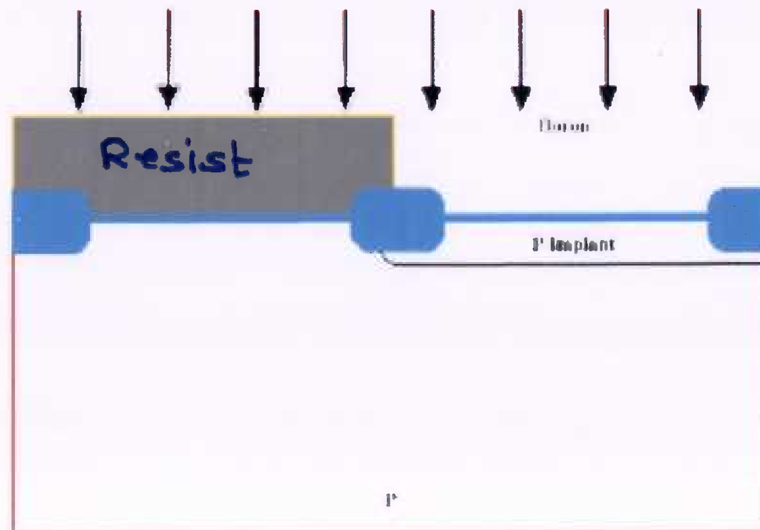


• **LOCOS**: after resist stripping the field oxide is grown using a Local Oxidation of Silicon process. Typical conditions are 1000°C, 90 min. in Wet ==> 0.5 micron oxide

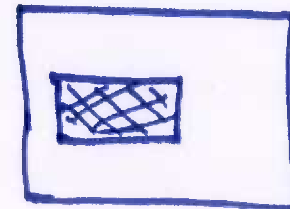
Strip Nitride layer.



• **P Well Formation:**
Mask #2 blocks a B+ ion implant to form the wells for the NMOS devices. Typical conditions are 10^{13} cm^{-2} @ 150 to 200 KeV (to yield final well concentration of ~ 10^{17} cm^{-3}).

PPR → Clear field Mask

P-Well Mask



Shallow Trench Isolation (STI)

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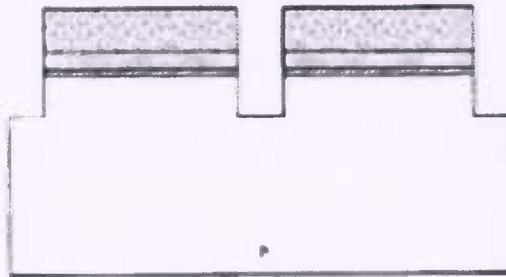
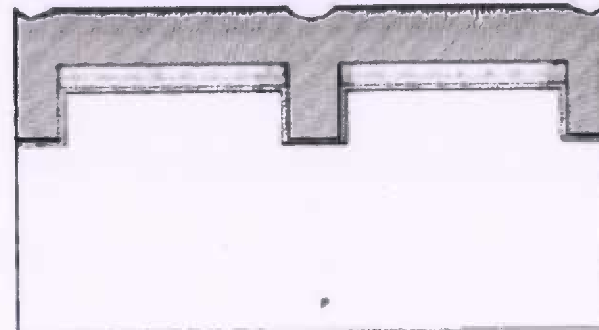
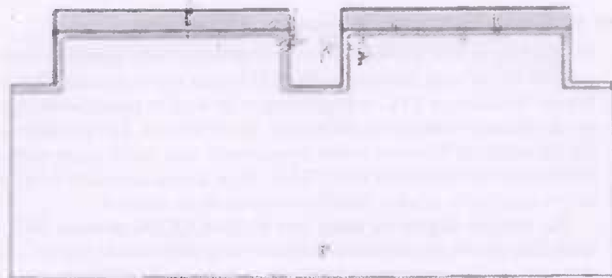
Outline of Shallow Trench Isolation (STI) Process (in place of LOCOS)

(1) After resist patterning, etch nitride, oxide, and ~ 0.5 micron deep Si trench



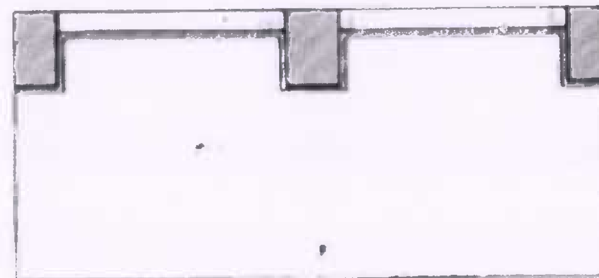
(3) CVD of thick SiO2 layer (requires good gap fill)





(2) Growth of thermal oxide 'liner' in the trenches. Nitride protects top of wafer surface.

(4) After CMP planarization



- minimal encroachment allows tighter packing of devices

Final N-Well and P-Well Creation

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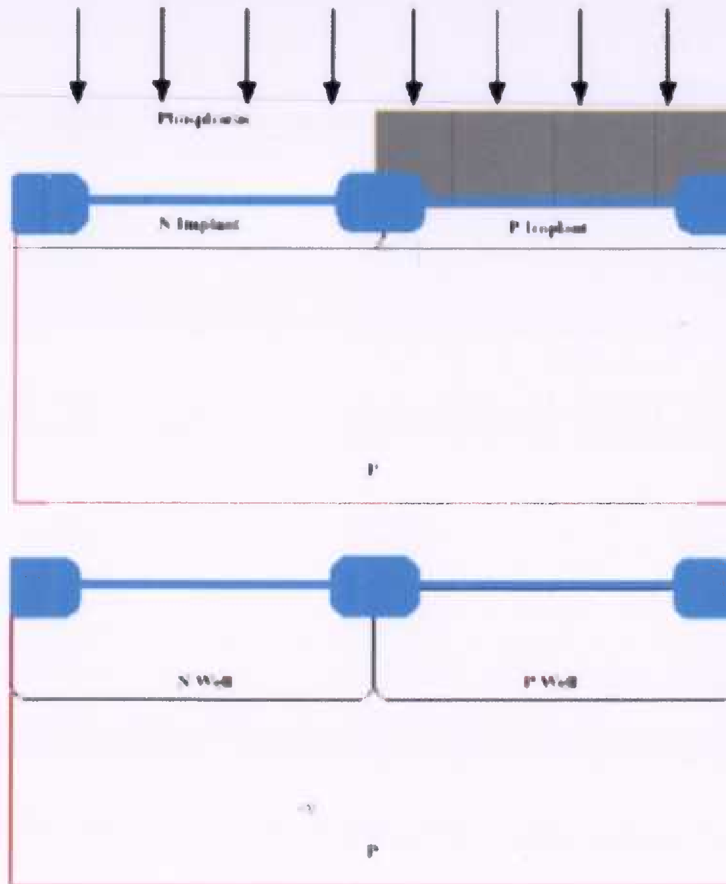
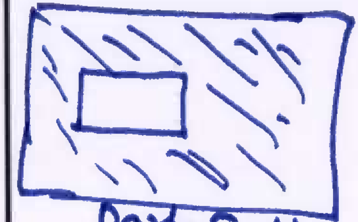
Continuation of Process Flow (LOCOS isolation example)



- **N Well Formation:**
Mask #3 blocks a Phos. ion implant to form the wells for the PMOS devices. Typical conditions: 10^{13} cm^{-2} @ 300 KeV. Note that As & Sb do not diffusion fast enough (and are too heavy) to form the N well. (P-well Minus)



- High temperature drive-in produces the **final well depths** and repairs implant damage. Typical conditions:
4 to 6 hrs. @ 1000 to 1100°C, or equivalent Dt.
$x_{well} \simeq 2\text{-}3\ \mu m$.

$$V_T = \phi_{ms} \pm 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{\pm Q_B}{C_{ox}}$$

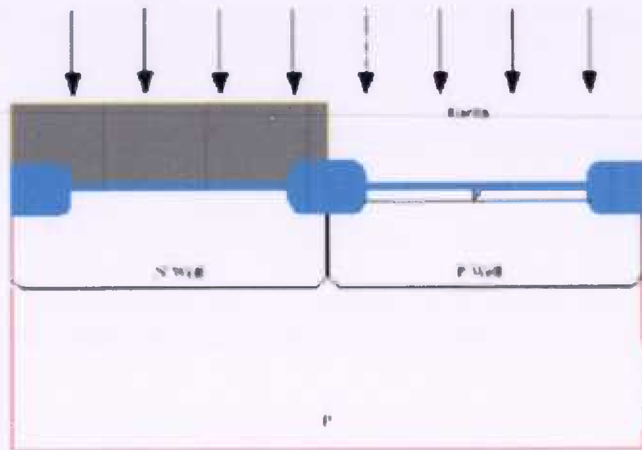
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$ $\rightarrow$ Gate oxide Thickness

$$Q_B = \pm q N_B x_{dmax} \qquad x_{dmax} = \sqrt{\frac{2 k_s \epsilon_0 (2\phi_F)}{q N_B}}$$

$$2\phi_F = \frac{2kT}{q} \ln \frac{N_a, N_d}{n_i}$$

Threshold V_T can be adjusted through 'Q_B'.

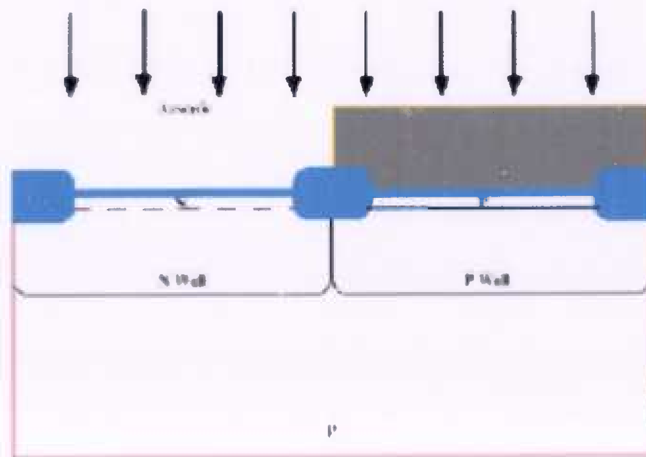
Threshold Adjust Implants



- **NMOS V_{TH} adjust**: Mask #4 is use to protect the PMOS devices. B is ion implanted to adjust V_{TH}. Typical conditions: 1-5 x 10^{12} cm^{-2}, 50 - 85 KeV.

$$\Delta V_T = \frac{Q_{implant}}{C_{ox}}$$

C_{ox} = Gate Oxide Cap/area.

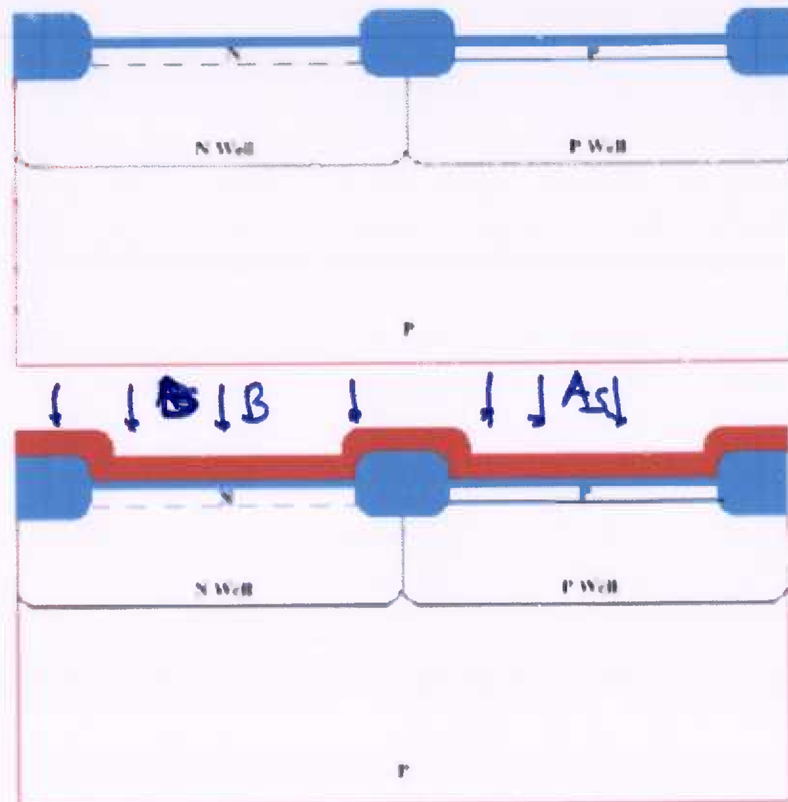


- **PMOS V_{TH} adjust**: Mask #5 is use to protect the NMOS devices. As^{+} is ion implanted to adjust V_{TH}. Typical conditions: 1-5 x 10^{12} cm^{-2}, 75 - 100 KeV.

Mask 4 & Mask 5 are complimentary

Polysilicon Gate Realization

Gate Stack Formation



- Etch back thin oxide and **grow clean gate oxide** ~ 5 nm, which can be grown at 800°C in ~ 1 hr.

Dry Oxidation

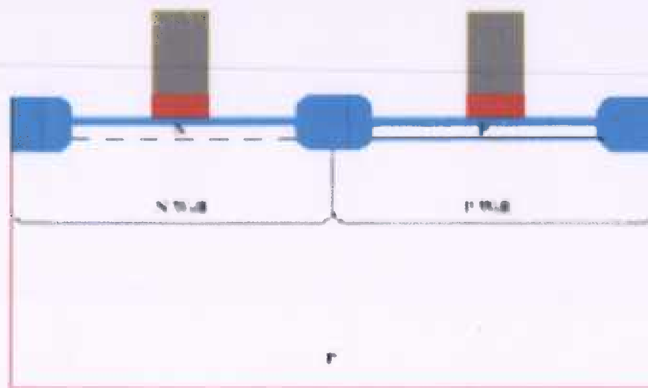
Nitrided oxides are typical today, and alternative high-K dielectrics are also being considered for sub 90 nm, Node

- LPCVD **polysilicon gate deposition** (~0.1 microns). Either masked or unmasked polysilicon doping implant is then performed (target dose such that final average poly doping is > 10^{20} cm^{-3}).

$R_s \simeq$ 10 – 20 ohm/□

Doping of Poly.
1. In Situ during Poly deposition
2. Solid State Diff.
3. Implant

Gate Delineation



• **Gate etch**: Mask #6 is used to protect the MOS gates. The polysilicon is plasma etched using an anisotropic etch which stops on the underlying oxide.

Process option: **gate re-oxidation** (to improve reliability in very thin gate oxide devices). Must be done carefully to avoid formation of non-uniform gate oxide thickness:

K. Rim, Ph.D. thesis, Stanford Univ.

S/D Extensions for SCE reduction

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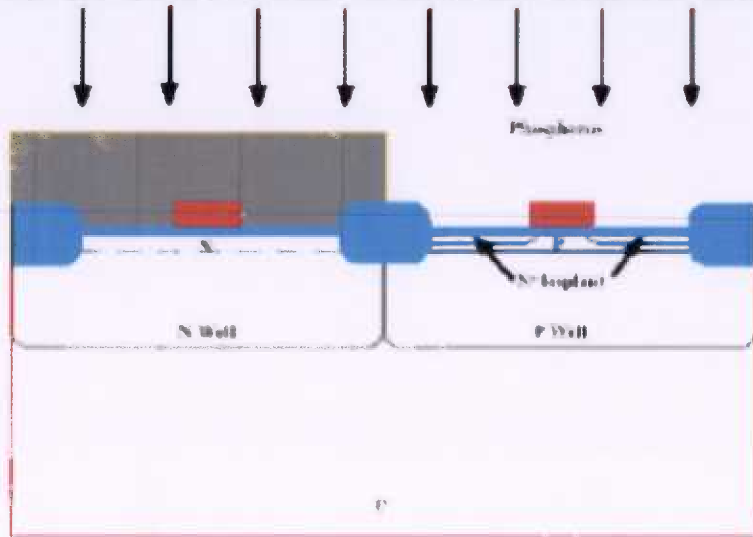
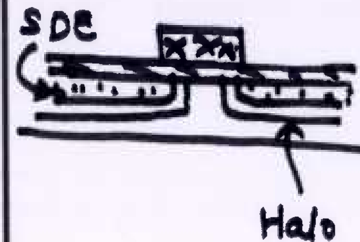
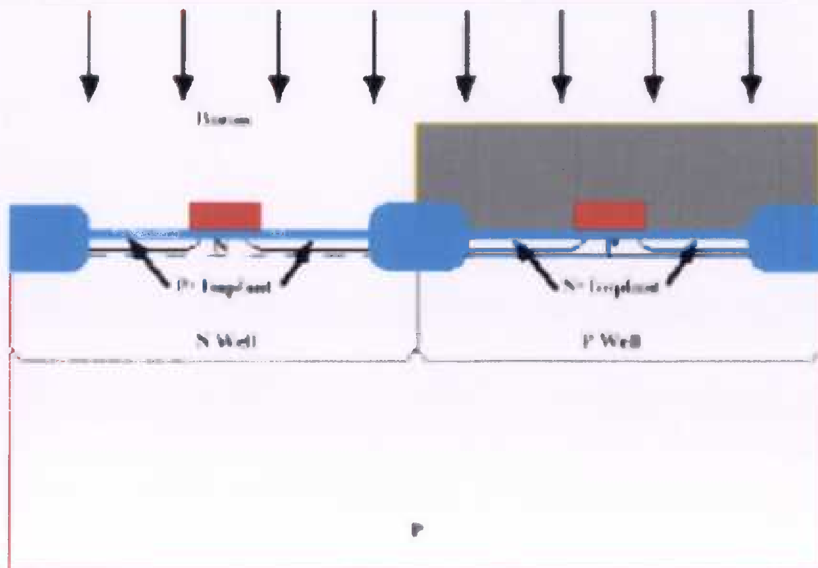


- **NMOS S/D Extension formation:** Original concept was Lightly Doped Drain (LDD) to help deal with hot electron effects. Today, the S/D extension serves to mitigate short channel effects. Mask #7 protects the PMOS devices. An As+ implant forms the LDD regions in the NMOS devices.





- **PMOS S/D Extension formation:** Mask #8 protects the PMOS devices. A B^+ implant forms the LDD or extension regions.

Sidewall Spacer creation

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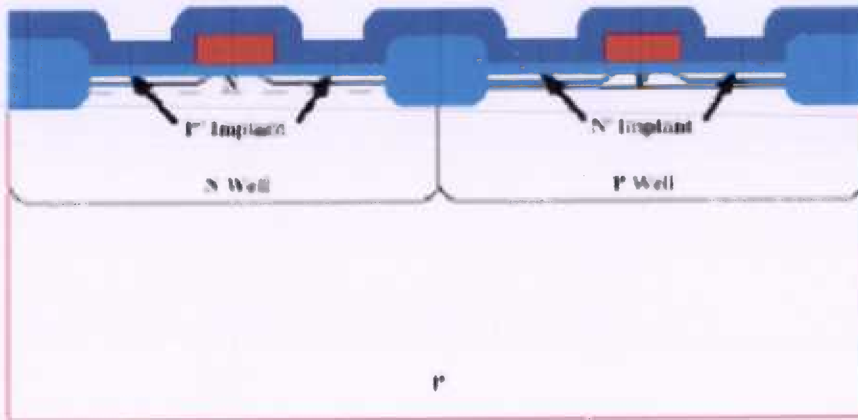
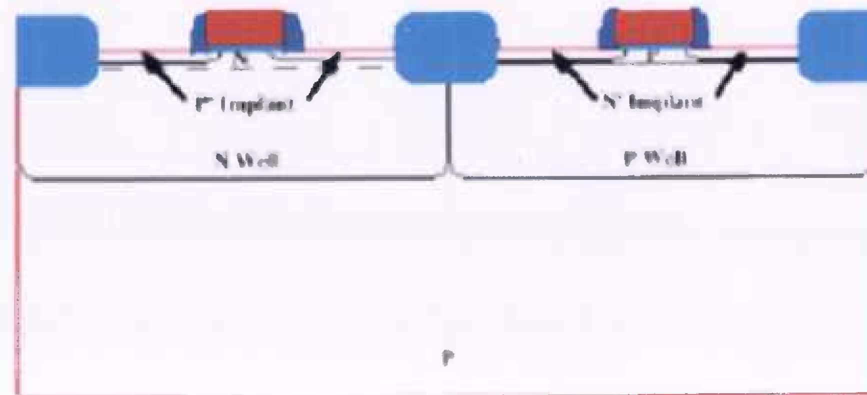


- **Sidewall spacer formation (oxide):**
A conformal layer of SiO_2 is deposited (typically ~ 0.1 to 0.25 microns thick) LPCVD Process.

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_2Cl_2 + N_2O \rightarrow SiO_2 + 2N_2 + 2HCl.$$



- **Sidewall formation:**
Anisotropic etching leaves behind "sidewall spacers" along the sides of the polysilicon gates.