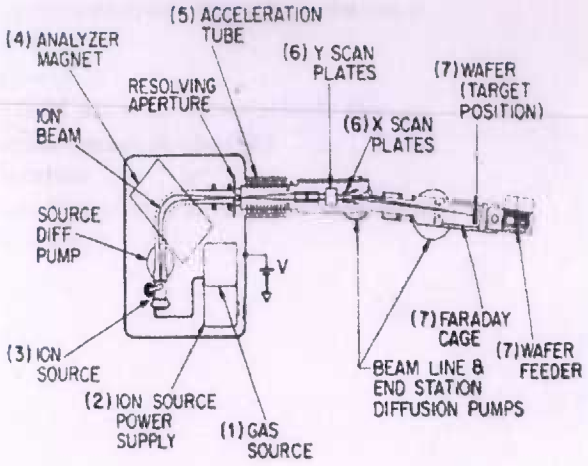
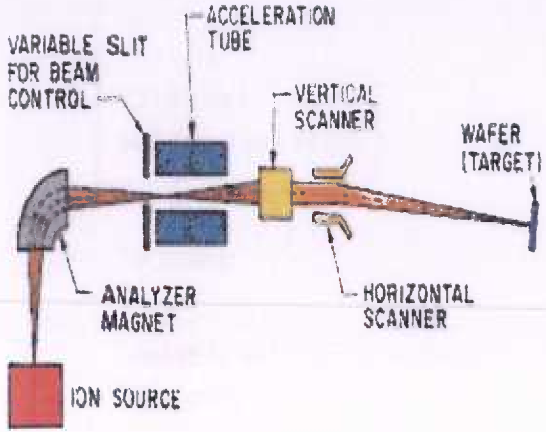
Selective doping - Ion Implantation-Machine

- (1) Gas source of material, such as BF3 or AsH3 at high accelerating potential; valve controls flow of gas to ion source
- (2) Power supply to energize the ion source
- (3) Ion source containing plasma with the species of interest (such as +As, +B, or +BF2), at pressures of ~ 10-3 torr
- (4) Analyzer magnet: allows only ions with desired charge/mass ratio through
- (5) Acceleration tube through which the beam passes
- (6) Deflection plates to which voltages are applied to scan the beam in x and y directions and give uniform implantation
- (7) Target chamber consisting of area-defining aperture, Faraday cage, and wafer feed mechanism



Ref: Dept of EE
Sherifa Technology
University, Iran

Selective doping - Ion Implantation



Principles of Ion Implant

- Generation of ions
  - dopant gas containing desired species
- BF3, B2H6, PH3, AsH3, AsF5
  - plasma provides positive ions
- (B11)+, BF2 +, (P31)+, (P31)++
- Ion Extraction
  - Ions are extracted from the source due to a high electric field
- Ion Selection
  - Magnetic field mass analyzer selects the appropriate ion (mass & charge)
- Ion Acceleration
  - Further accelerate ions giving the ions their final kinetic energy.

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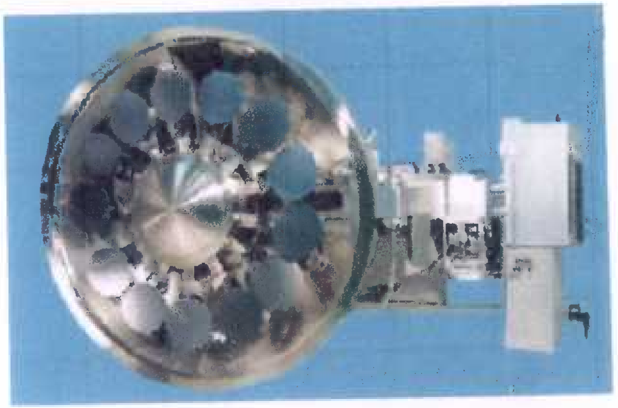
L-21 slide-03

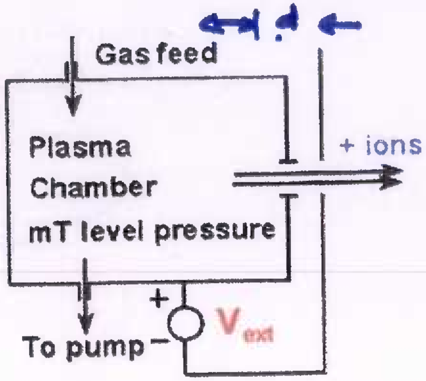
Selective doping - Ion Implantation



Multi-Wafer chuck

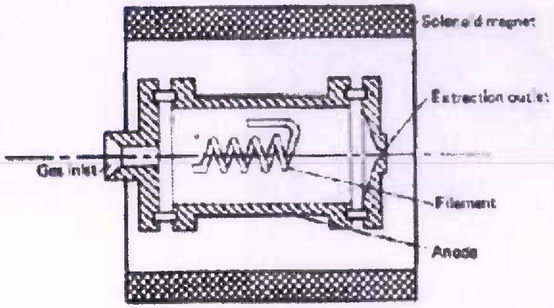
Ref :- Deptt of EE
STU, Iran

Selective doping - Ion Implantation-
Plasma source



variable extraction voltage
(typically ~30KV)

Nielsen-type gaseous source



Pressure : 10^{-4} to 10^{-2} Torr

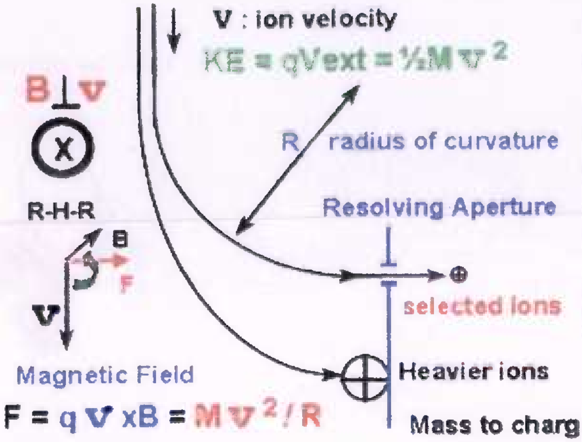
Ion source is characterised by

Ion current density

$$J_{ion} = \frac{5.5 \times 10^{-8} V_{ext}^{3/2}}{d^2 \cdot M^{1/2}} \text{ Amp/cm}^2$$

Ref : Dept of EE
STU, Iran

Selective doping - Ion Implantation-Mass analyzer



The ions are extracted from the source and analyzed in a magnetic field. The Lorentz force makes the ions take a curved path with a radius of curvature that depends on the mass of each ionic species. By adjusting the magnetic field strength, only the selected ions will enter the accelerating column.

Mass to charge ratio of the selected ions:

$$\boxed{M/q = R^2 B^2 / (2 V_{ext})}$$

v = velocity

R = Radius of Curvature.

$$v = \sqrt{\frac{2q}{m} V_{ext}}$$

$$B \cdot R = \sqrt{\frac{2q}{m} V_{ext}} \Big/ (q/M)$$

$$= 4.55 \sqrt{M V_{ext}} \quad \text{KG.cm}$$

B.R is called Magnetic Rigidity.

Conclusion:

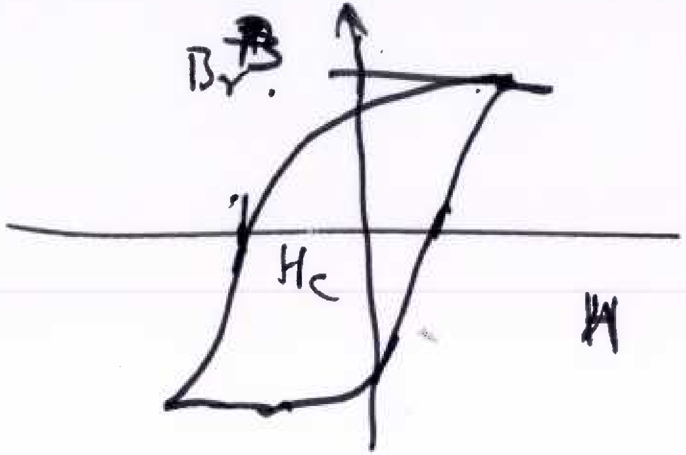
For a Magnet, R is Fixed.

Hence for a given Extractor Voltage

$$B \propto \sqrt{M}$$

B is Controlled by Coil Current, which can then fix species of One Mass.

Ref: Deft of EE, STU, Iran



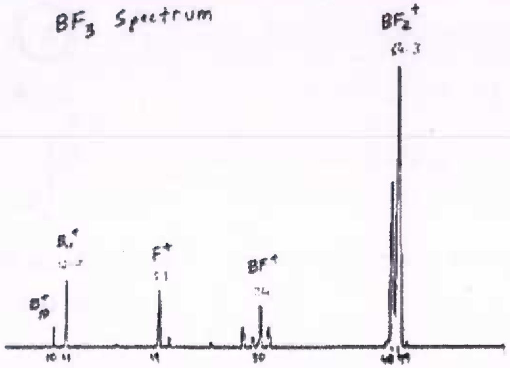
Hysterisis is seen in B-H curve of Magnets

Magnetisation Curve for a Magnet

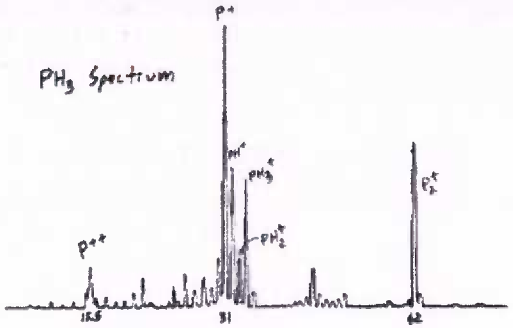
1 Parmanent Magnet
2. Electromagnet
3. Temporary Magnet

Selective doping - Ion Implantation- Mass analyzer

BF_3 Gas Spectrum



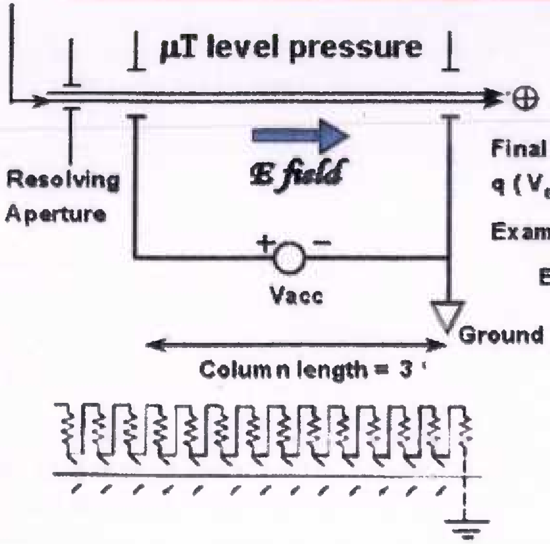
PH_3 Gas Spectrum



Ref:- Dept of EE
STU, Iran

Selective doping - Ion Implantation- Accelerator

Ion Acceleration



Final Kinetic Energy of the Ion = $q\,(V_{ext} + V_{acc})$

Example: V_{ext} = 30 KV V_{acc} = 70 KV

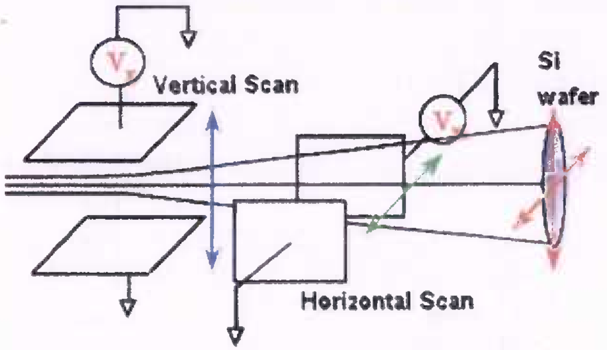
Energy of the Ion = 100 KeV

Ref Dept of EE
STU, Iran

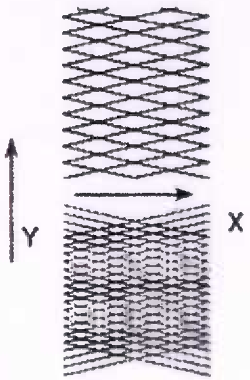
Selective doping - Ion Implantation- Scanner

Beam Scanning

Electostatic scanning (low/medium beam current implanters ($I < 1mA$)



Scan Patterns

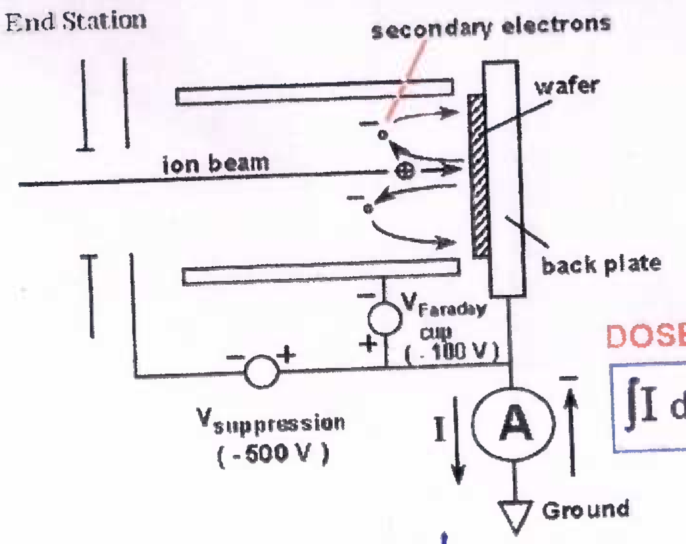


This type of implanter is suitable for low dose implants. The beam current is adjusted to result in $t > 10$ sec/wafer. With scan frequencies in the 100 Hz range, good implant uniformity is achieved with reasonable throughput.

Ref: Dept of EE
STU, Iran

Selective doping - Ion Implantation-Wafer cage (Faraday Cup)

In-situ Dose Control



DOSE MONITORING

$\int I\, dt = Q = A q \phi$

$$N_s = \text{Dose} = \frac{1}{qA} \int_0^{t'} I(t)\, dt$$

Ref:- Dept of EE
Sharifa Technology
University, Iran

Silicon Integrated Circuit Process Flow for CMOS Technology

CMOS PROCESS FLOW (BASIC PROCESS)

1. Choice of Substrate :

MOS CIRCUITS :— <100> Oriented
Bipolar Circuits :— <111> Oriented

(ii) Doping : 5-50 Ω cm

(iii) P-type (Boron) Doped Wafers

Typical Conc. $\hat{=} 10^{15}$/cc for 0.25μ Technology Node

EDP count $< 1/cm^2$

(iv) Wafer Size & Thickness as per Technology Node.

2. Active Area Creation:

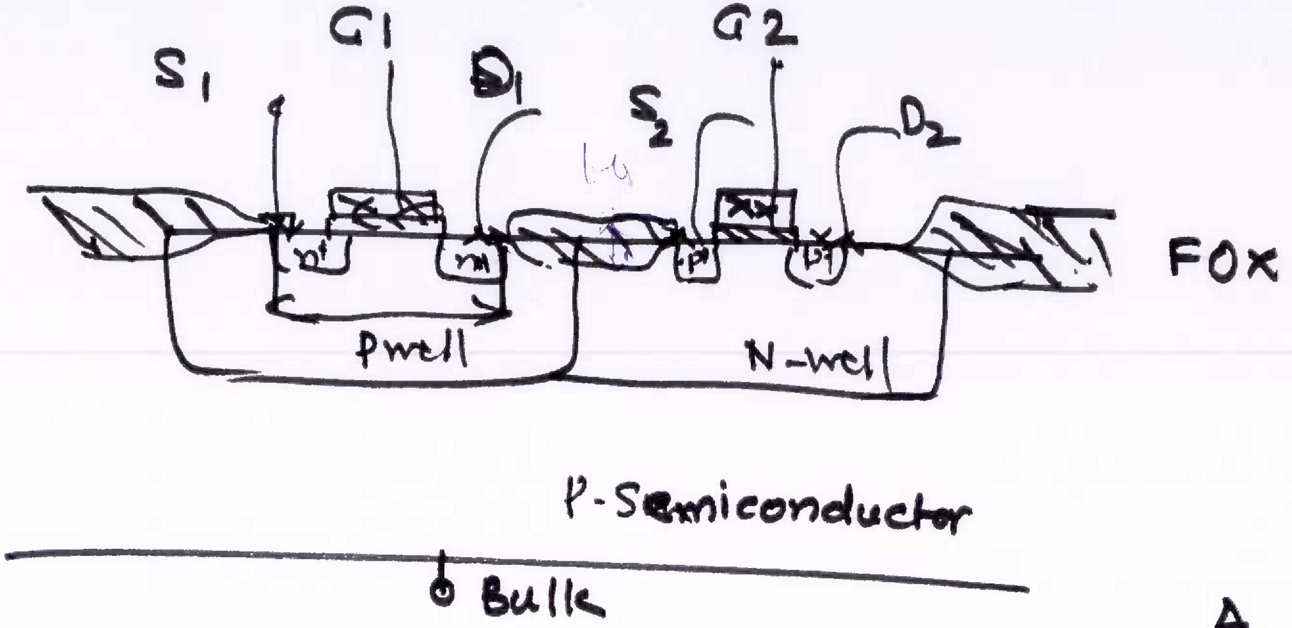
Active areas are those regions where MOS Transistors will be created.

All transistors need to be separated and Process which allows this is called 'Isolation'. '1st Mask' is used here to delineate Active areas, and hence called "Active Area Mask".

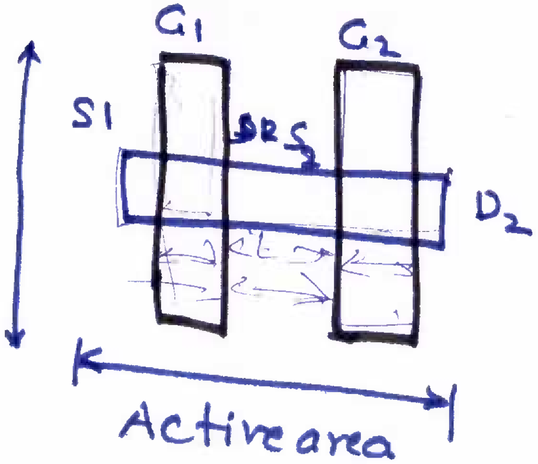
Isolation is provided by thick Oxide and there are two ways it is created in an MOS ICs.

(i) LOCOS Process used to create Bird's Beak or Bird's Crest.

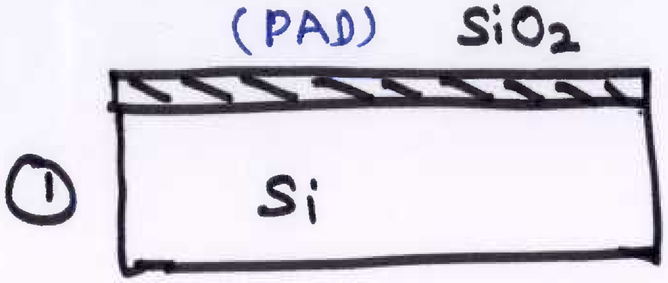
(ii) LOCOS is used to create "Shallow Trench Isolation" also popularly called 'STI'

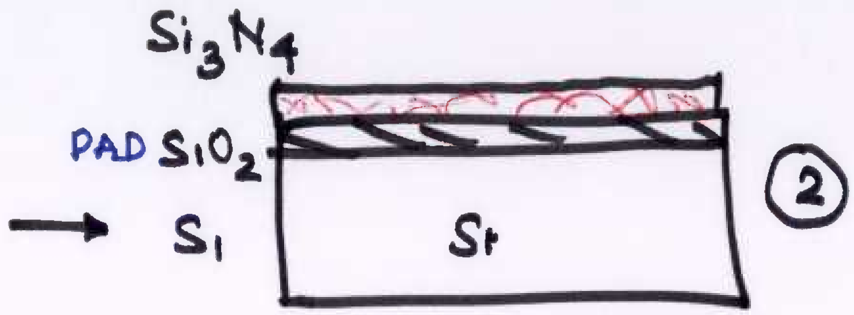


A Typical basic CMOS transistor Cross-section



Mask for above figure





Thermal Growth

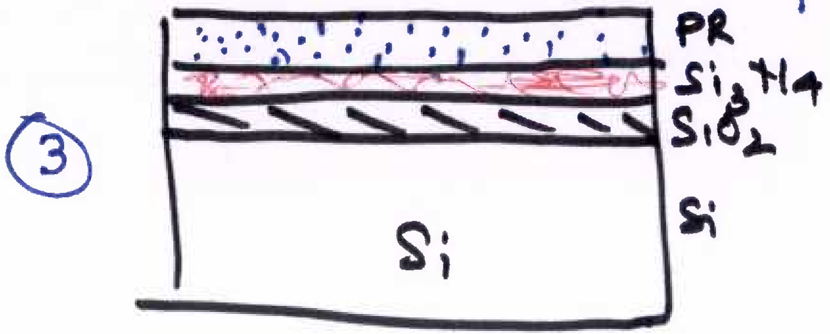
$Si + O_2 \rightarrow SiO_2$ (~ 40nm)

Si_3N_4 Deposition

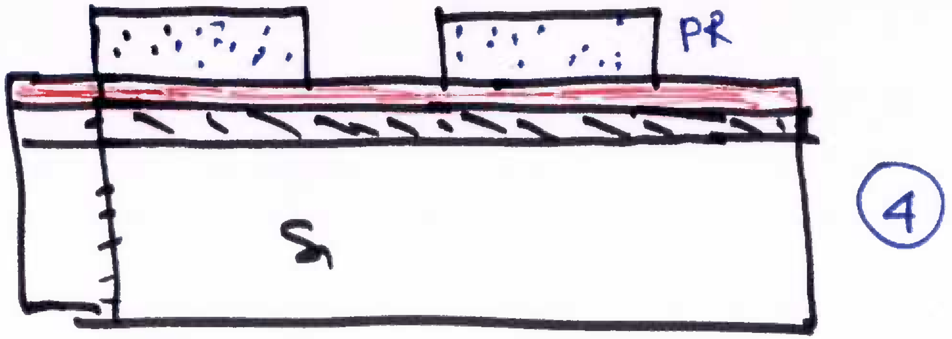
$$3\,SiH_4 + 4\,NH_3 \xrightarrow[800^\circ C]{LPCVD} Si_3N_4 + 12\,H_2$$

Typical Thickness (800 Å)

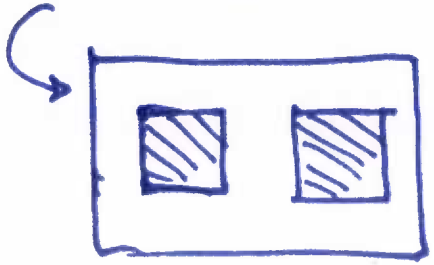
Photoresist (Deposition + Spin)



Photoresists thickness
0.6 µm to 1.0 µm

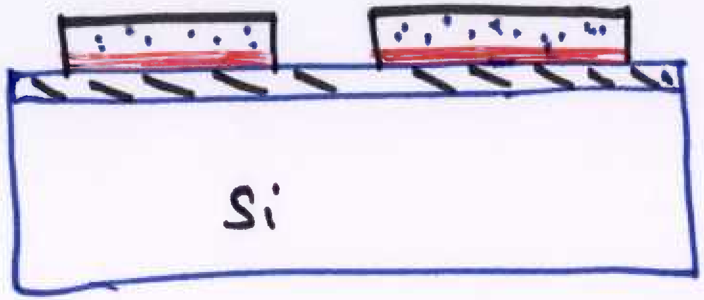


Ist Mask — Lithography



Clear field
for PPR

⑤

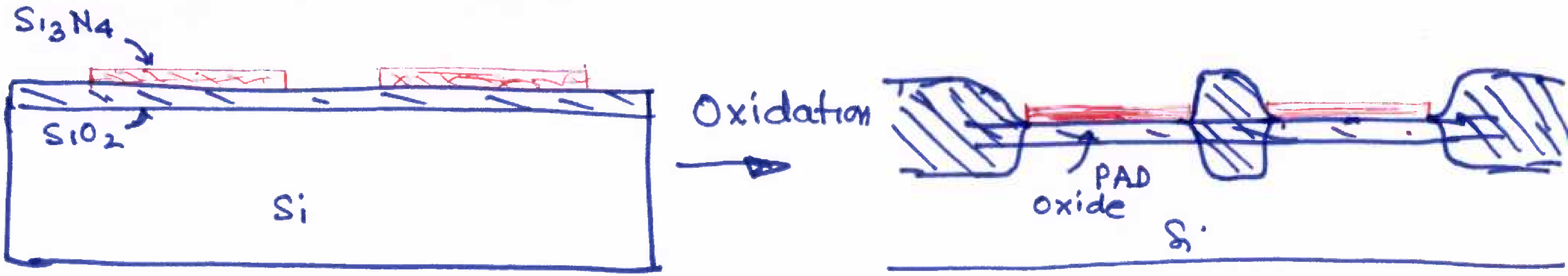


Pattern etched in Photoresist (Development) and Silicon Nitride

$$Si_3N_4 + 12F \xrightarrow[\text{Etching}]{} 3SiF_4 + 2N_2$$

Keeping Resist & Si_3N_4 in areas which are active areas

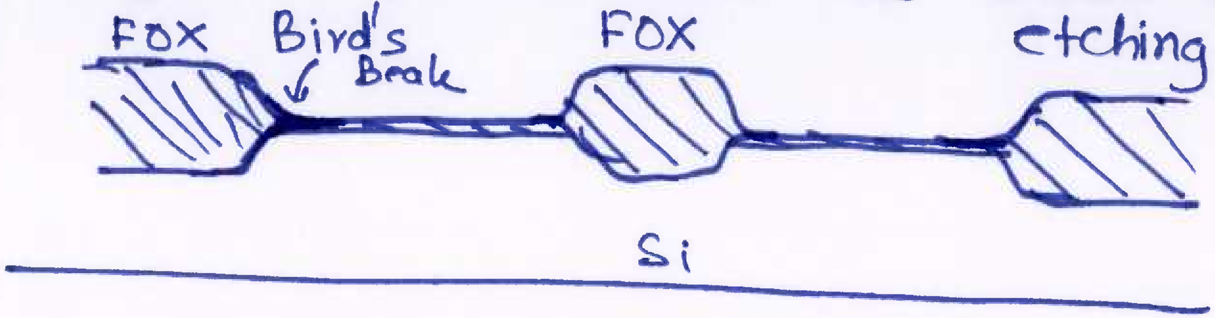
Then Resist is Stripped

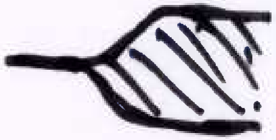


LOCOS

Dry - Wet - Dry Oxidation

Magnified pattern looks like Bird's Beak after etching Si_3N_4





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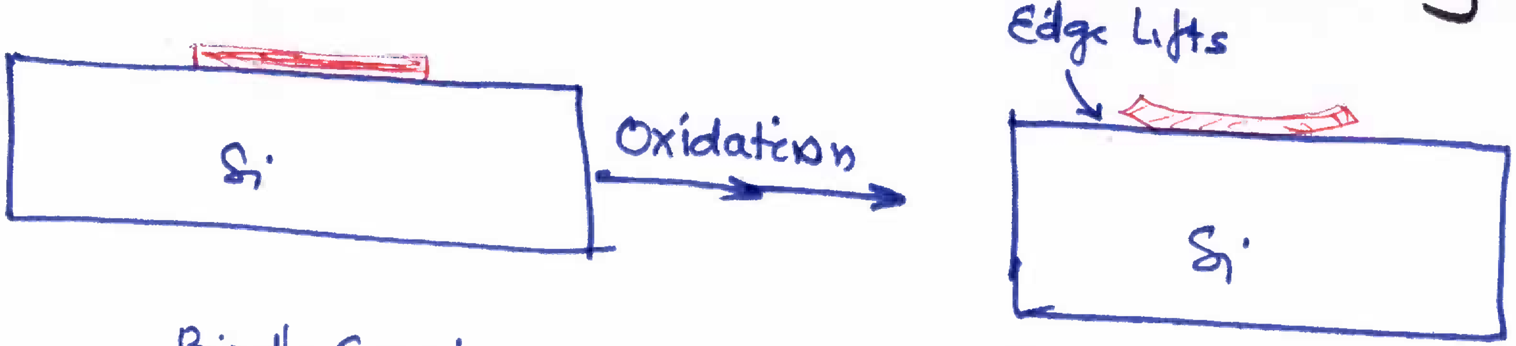
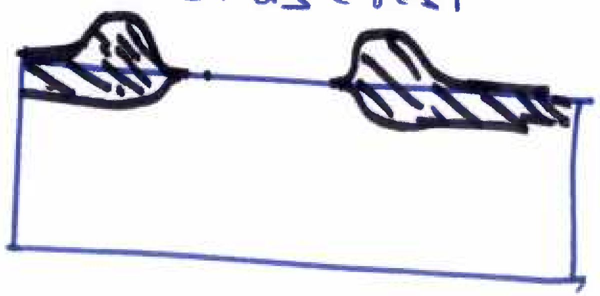
If we donot have Initial 'PAD-oxide', but directly deposite Si Nitride, then we see. after Patterning we have



Bird's Crest

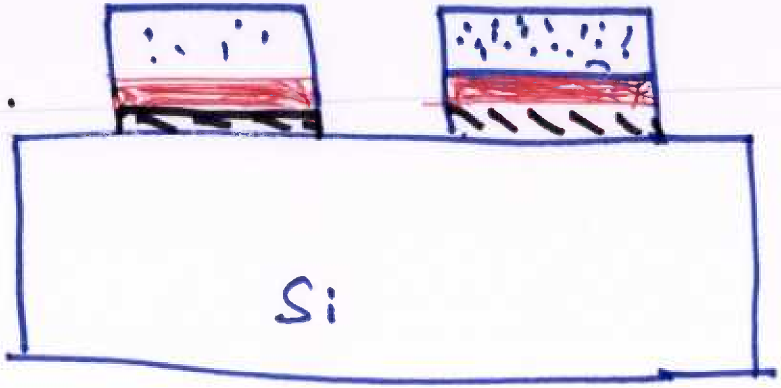


Due to Mismatch of Thermal Coeff. of Expansion, Si_3N_4 lifts from edges during patterning & removal of resist followed Thermal Cycle

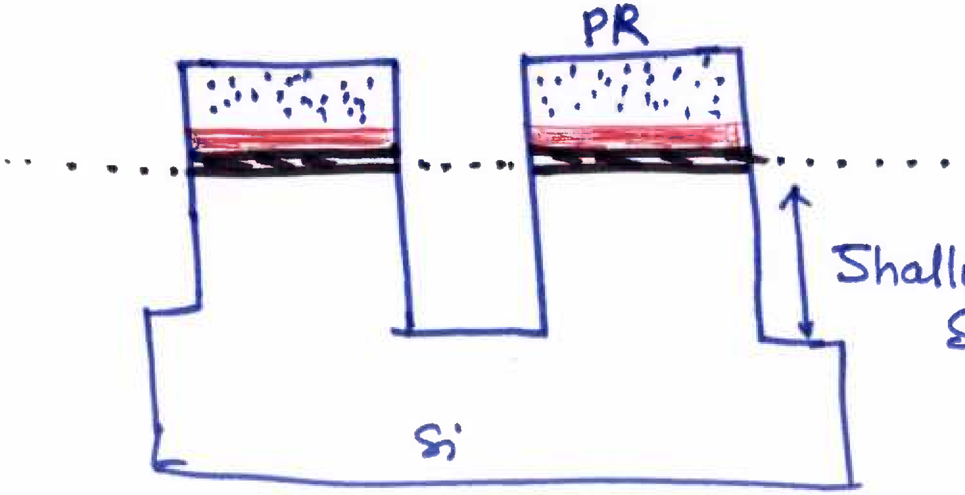
After Oxidation Si_3N_4 is etched out -

Shallow Trench Isolation (STI)

First ④ steps are identical to normal LOCOS Process. Even 5th step is also same.



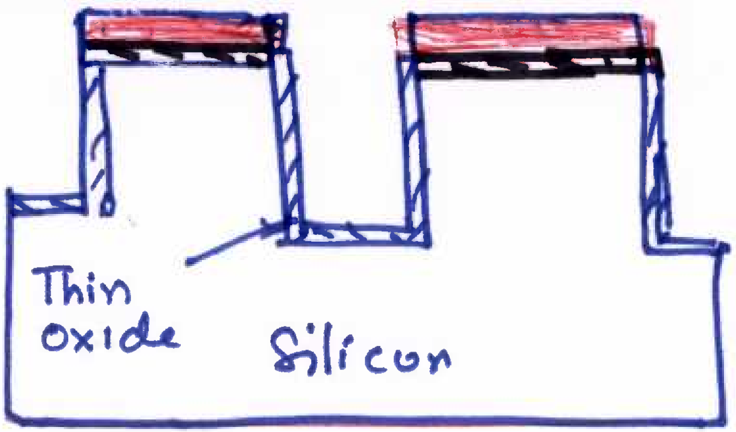
Now we do Silicon etching through created windows



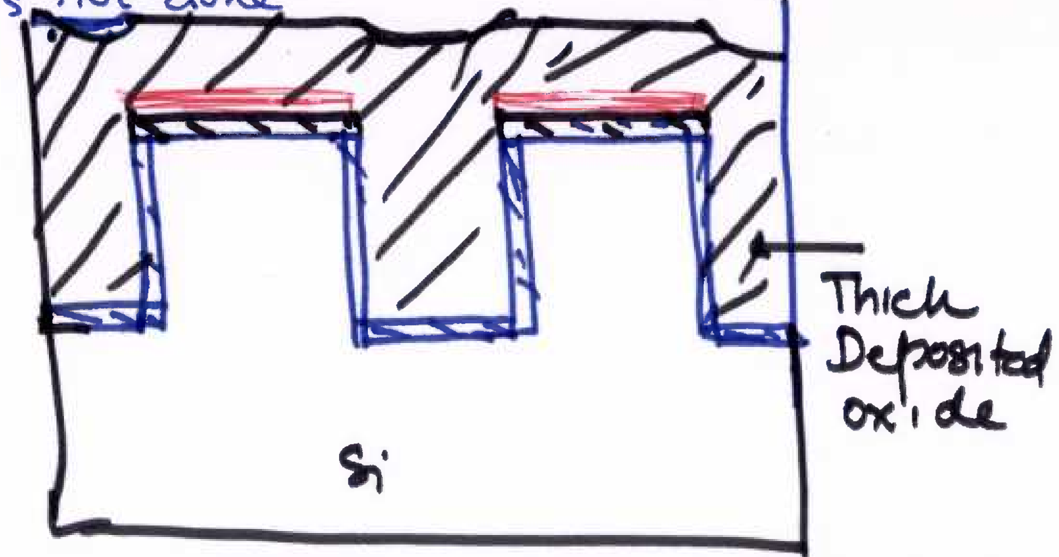
After etching of Trenches in Silicon, one removes resist by Stripping.

Then wafers are subjected to Dry Oxidation for creation of good quality thin layers on all sides of Trenches. Oxide thickness is around 100 Å to 200 Å.

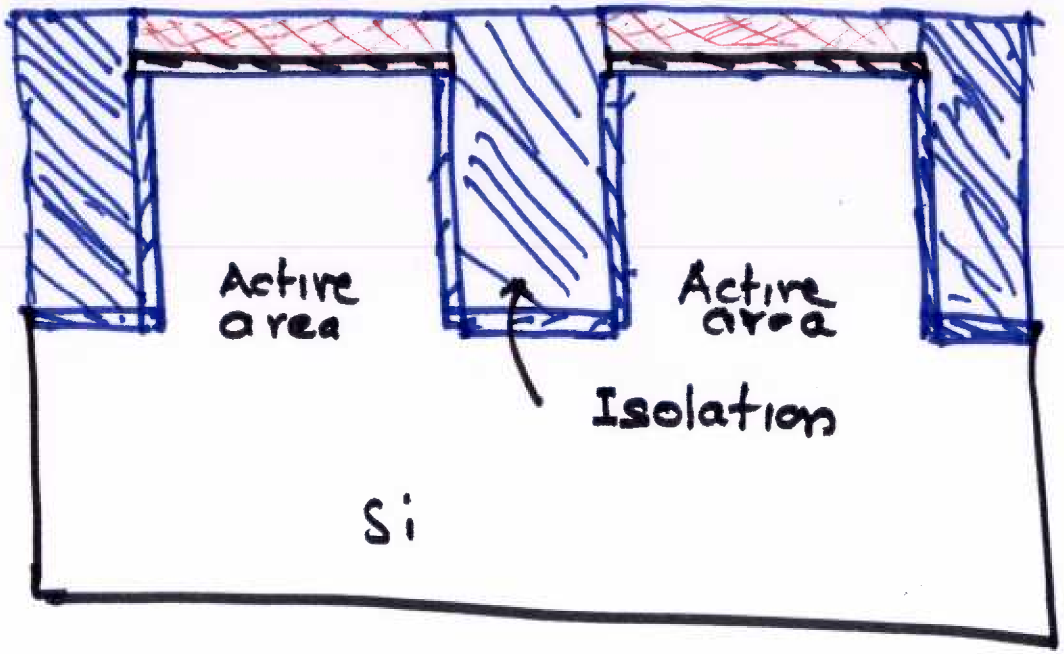
The wafer status is shown below.



Then Thick Silicon Dioxide is Deposited after Removal of Si_3N_4 or many a times This is not done



Now Upper Surface which has undulation, is given Chemical Mechanical Polish (CMP), which planerises that top layer.



Recessed Trenched Oxide Isolation (STI)