"Lithography"

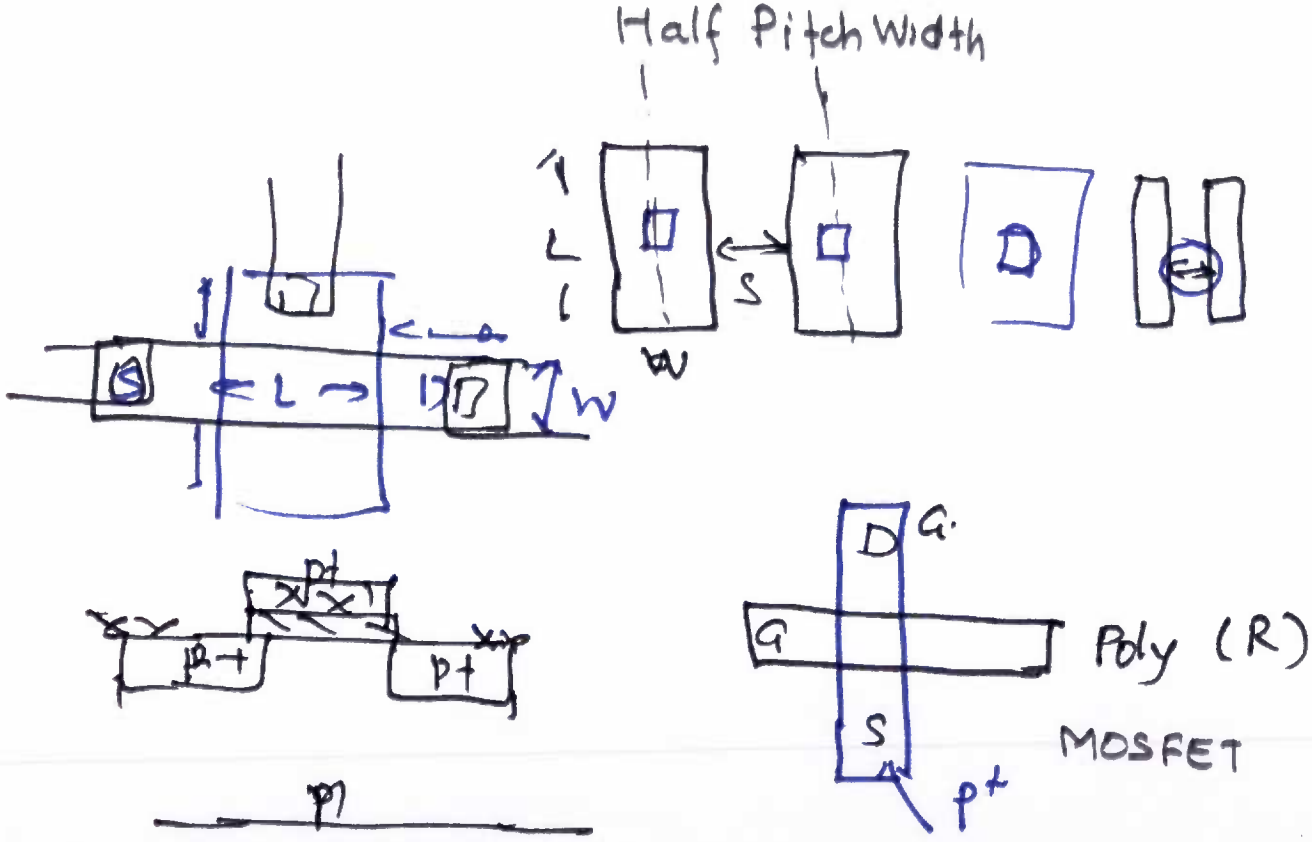
(i) Photolithography

(ii) e-Beam Lithography

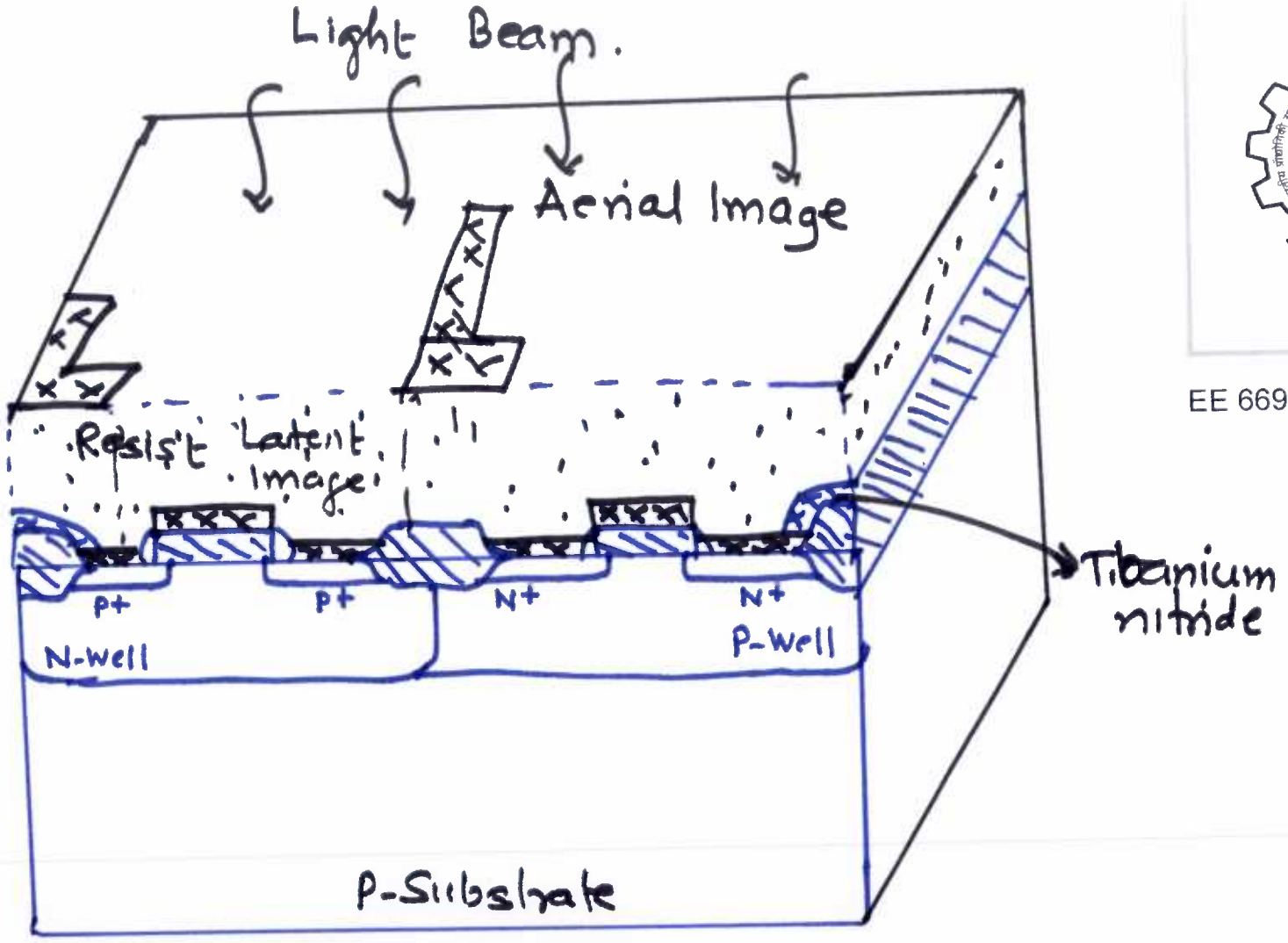
(iii) X-ray Beam lithography

"Pattern Transfer Techinque"

1. Mask
2. Etching



Cross-Section & Layouts



CMOS PROCESS

Lithography is the process that creates features on a silicon wafer to form an Integrated Circuit.

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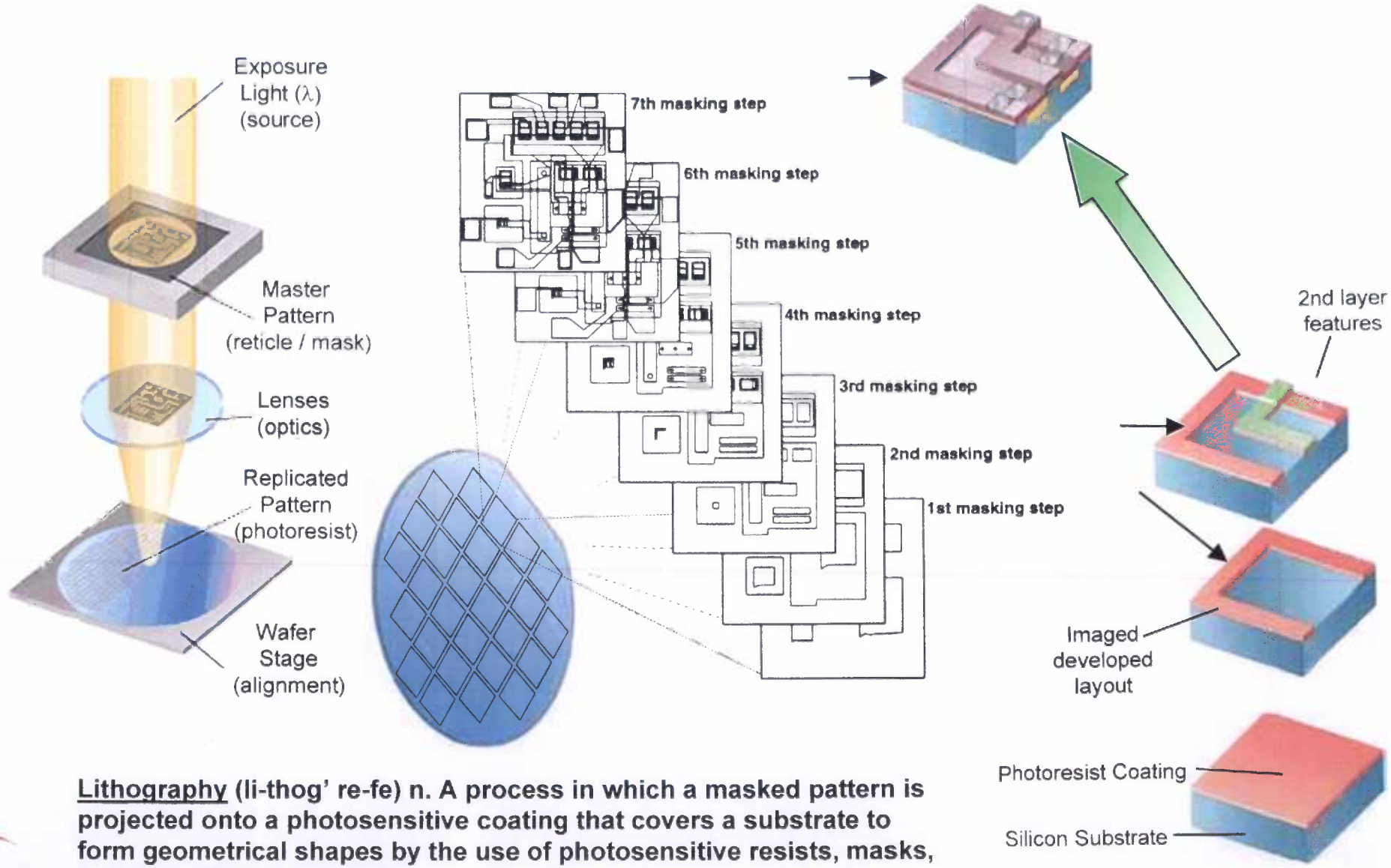


Lithography (li-thog' re-fe) n. A process in which a masked pattern is projected onto a photosensitive coating that covers a substrate to form geometrical shapes by the use of photosensitive resists, masks, and developing techniques

INTERNATIONAL SEMATECH

Integrated Circuits could only be realised due to a most important Process called Lithography.

Moore's Law was essentially based on improvements in lithography

Roughly $(1/3)^{rd}$ of the cost of IC manufacture goes into Lithography.

Lithography is the technique of transferring Layout Patterns on Silicon and allow selective etching as per pattern.

Three issues of lithography are

(i) Mask Design

(ii) Mask Fabrication

(iii) Wafer Printing

(i) Mask Design :—

From a Circuit performance of an IC, we realise All Process-Levels Masks and they are then used in selective area processing.

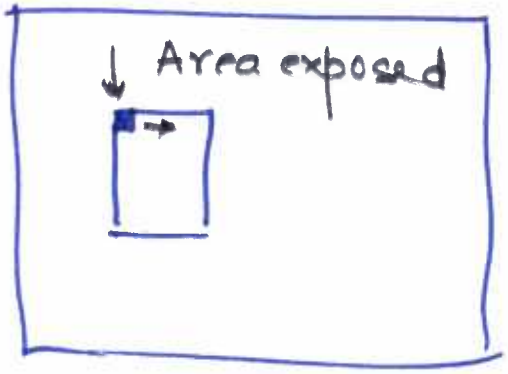
Layouts are given in the form of 'gds' format which essentially represents the coordinates of each pattern. There could be 16 or more Numbers of Masks Patterns. Before they could be used, these Patterns are made first on Mask Plates.

From CAD tool use, we create layouts, and then use Back Extraction to get Circuit Schematic. Circuit Simulations prior and after 'Layout' need to be matched. Further Layouts are also subjected to DRCs, before they are committed to 'Mask Plates'.

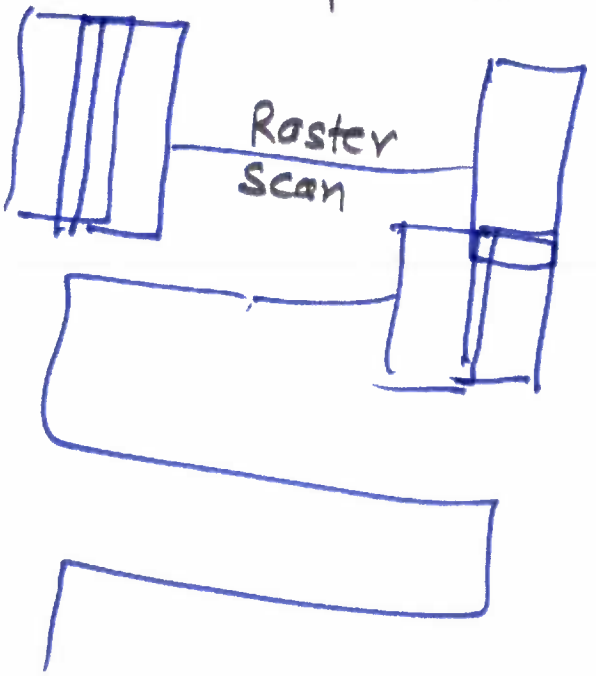
Mask-Making System uses a Microscope like systems which transfers images on photoemulsion plates.

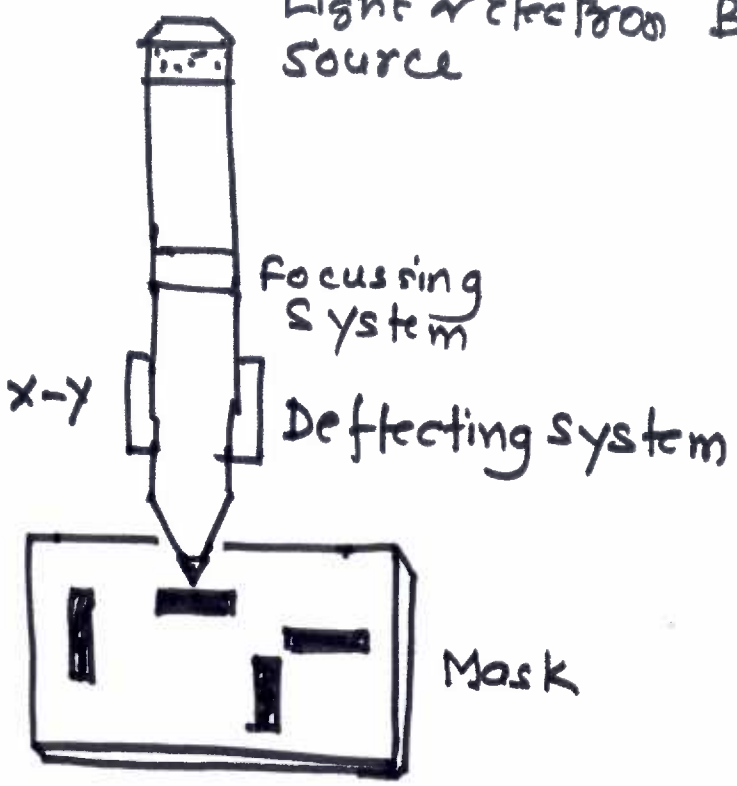
One Single Pattern of a Circuit, needs to be replicated to large number of chips on a wafer. Thus we need a System which is called 'Step & Repeat'.

Mask making in Step & Repeat System



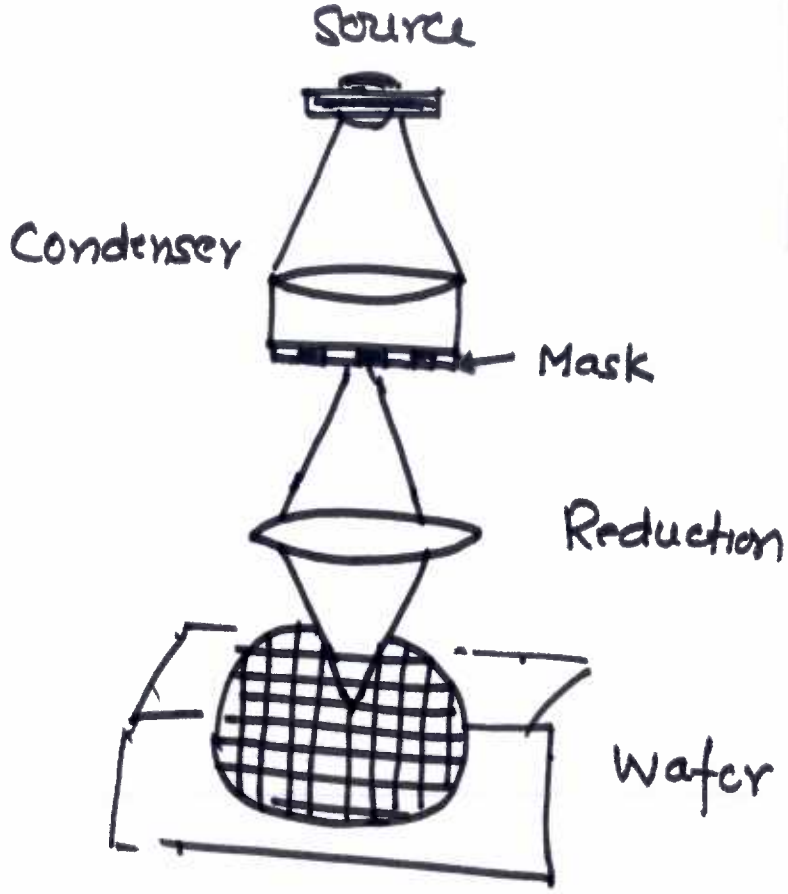
Overlap Exposure





Step system.

4x or 5x initial Pattern is reduced to X in Repeat system



Repeat System.

LIGHT SOURCES

Scale down technologies, will have smaller Features. To create Smaller dimension patterns, one needs Shorter Wavelength of beams.

Two Possible Sources : (a) Mercury atoms

(b) Electron Beams

i Photolithography — Light source — Hg vapour lamps as Source

ii Electron Beam Lithography — Electron Source — CRT like System

(i) Light Source uses lamp which has vapour pressure of the order of 20 to 40 Atm. This creates Plasma (High Intensity) which radiates many Spectral Lines.

In Plasma, effective electron temperature 40K °k.
Hence emission could produce UV and even deep UV.

In olden days $\lambda \cong 2900 \underset{-4000}{\text{Å}}$ was used. Now we have two spectral lines in use.

(a) g-line with $\lambda = 436$ nm (4360 Å)

(b) i-line with $\lambda = 365$ nm (3650 Å)

Best of features which can be delineated are known to be $0.25\mu - 0.35\mu m$.

Alternate to Plasma based UV system, one can use Excimer Lasers with high high Brightness.

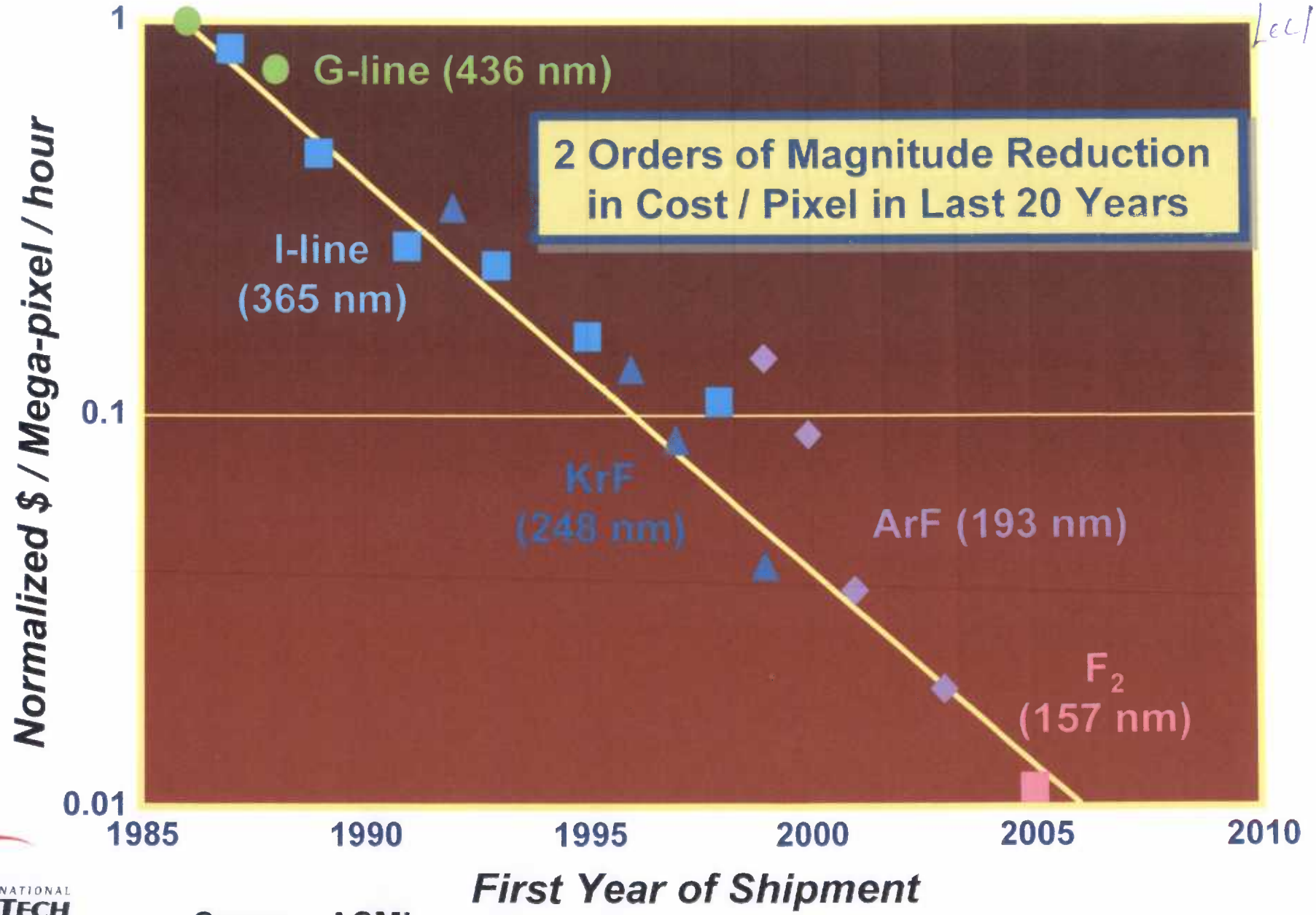
$$K_r + NF_3 \xrightarrow[\text{Energy}]{} K_rF \longrightarrow \text{Photons}$$

(a) K_rF – $\lambda = 248$ nm (Used for Technologies 0.13μ to 0.25μ)

(b) A_rf – $\lambda = \underline{193\text{ nm}}$ (Used for Technologies < 90 nm.

(c) CaF is also currently being Investigated.

Cost/Pixel Reduction for Optical Lithography



Source: ASML