Multiple Choice Questions

- 5.1 For each of the following cases identify the context if it is human $\leftarrow \rightarrow$ computer / device $\leftarrow \rightarrow$ computer or computer $\leftarrow \rightarrow$ computer communication:
 - a. Key board
 - b. Monitor
 - c. Touch screen
 - d. Joy stick
 - e. Floppy
 - f. CD drive
 - g. Modem
 - h. Broadband
- 5.2 For each of the following mechanism identify if it is human ← → computer / device ← → computer or computer ← → computer communication:
 - a. Polling
 - b. Read / write under program control
 - c. DMA
- 5.3 The programmed mode of IO is a blocking IO
 - a. True
 - b. False
- 5.4 We describe a protocol of input device communication below.
 - a. Each device has a distinct address
 - b. The bus controller scans each device in sequence of increasing address value to determine if the entity wishes to communicate.
 - c. The device ready to communicate leaves it data in IO register.
 - d. The data is picked up and the controller moves to step-a above.

Identify the form of communication best describes the IO mode amongst the following:

- a. Programmed mode of data transfer
- b. DMA
- c. Interrupt mode
- d. Polling

- 5.5 From amongst the following given scenarios determine the right one to justify interrupt mode of data-transfer:
 - a. Bulk transfer of several kilo-byte
 - b. Moderately large data transfer but more that 1 KB
 - c. Short events like mouse action
 - d. Key board inputs
- 5.6 Which of the following can be nested interrupts:
 - a. Soft-ware interrupts
 - b. Hardware interrupts
 - c. External interrupts
- 5.7 DMA is set up using an interrupt
 - a. True
 - b. False
- 5.8 Suppose a DMA is set up to transfer 100KB data. Identify which of the following statements are true.
 - a. The processor is interrupted after every byte of transfer
 - b. The processor interrogates at the end of every clock cycle if the transfer is complete
 - c. The DMA transfer the data independent of processor till the transfer is completed.
- 5.9 A Double buffer is a cyclic buffer with cycle length of 2
 - a. True
 - b. False
- 5.10 Who amongst the following sets the timer for preemptive scheduling:
 - a. The user
 - b. The processor clock
 - c. The operating system scheduler
- 5.11 IO channels are merely communication wires with no buffers
 - a. True
 - b. False

- 5.12 Put the following disk scheduling policies in the order that will result in minimum amount of head movement.
 - a. FCFS
 - b. Circular scan
 - c. Elevator algorithm