Elite

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This certificate is awarded to

MATCHA SAI POOJITHA

for successfully completing the course

VLSI Design Flow: RTL to GDS

with a consolidated score of **73** %

Online Assignments	24.38/25	Proctored Exam	48.22/75

Total number of candidates certified in this course: **4369**

Prof. Sumit J. Darak
Dean of Academic Affairs,
IIIT Delhi

Jul-Oct 2025

(12 week course)

Prof. Andrew Thangaraj
NPTEL, Coordinator
IIT Madras

INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

FREE ONLINE EDUCATION swayam शिक्षित भारत, उन्नत भारत

Roll No: NPTEL25EE106S572401779

To verify the certificate

No. of credits recommended: 3 or 4