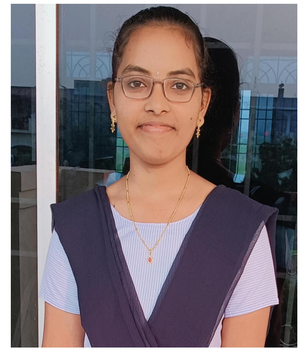
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This certificate is awarded to

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for successfully completing the course

System Design Through Verilog

with a consolidated score of **75** %

Online Assignments	20.92/25	Proctored Exam	54/75

Total number of candidates certified in this course: **2329**

Jul-Sep 2024

(8 week course)

Prof. T. V. Bharat
Head, Centre for Educational Technology
NPTEL Coordinator, IIT Guwahati

Indian Institute of Technology Guwahati

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